

Vegas Schematic

KBL-R

2017/11/08

REV : A00

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DY : None Installed

UMA: UMA only installed

OPS: DISCRTE OPTIMUS installed

<Core Design>



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Title

Cover Page

Size
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Document Number

Vegas SKL/KBL-U

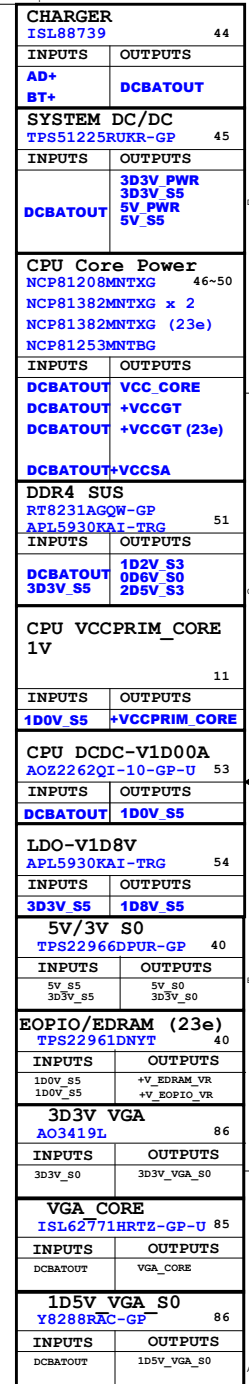
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A00

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Sheet 1 of 105

Vegas/Turis MLK KBL-R Block Diagram



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Document Number

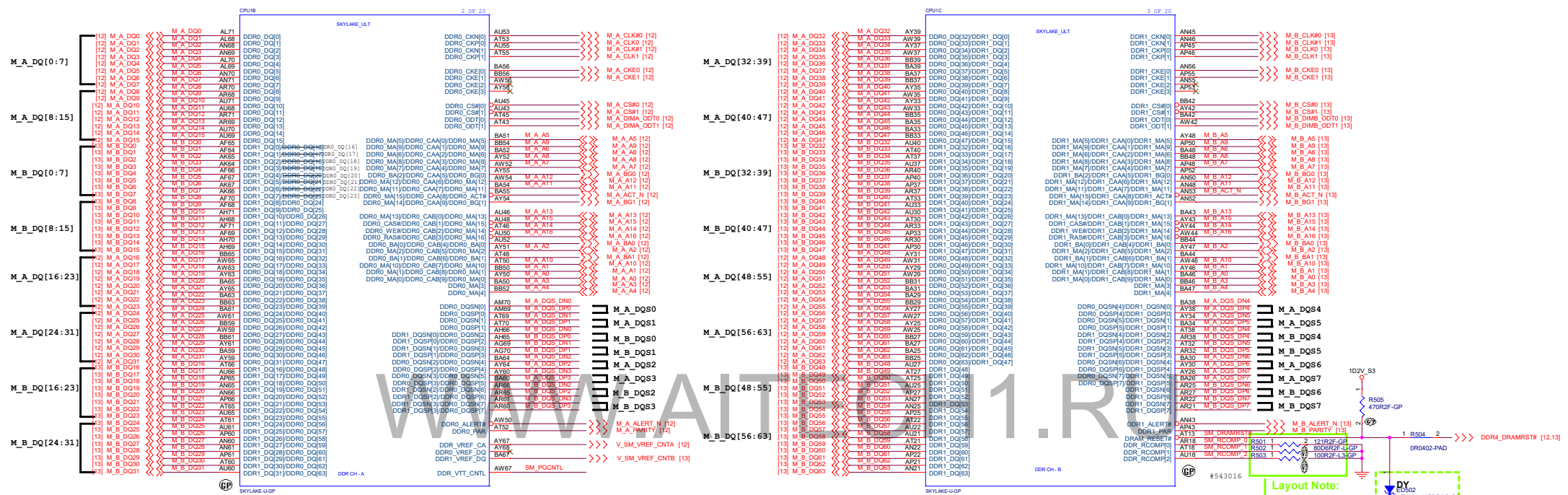
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DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel. Clock (CLK and CLKB) and Strobe (DS0 and DS0#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock swapping within a channel is not allowed.

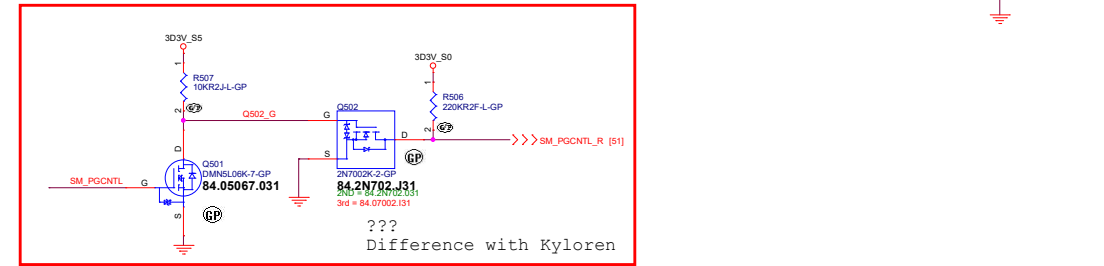
PDG: DDR/ODT

4.17 SKL U and SKL Y System Memory ODT Signal Connectivity Details

Table 4-41. ODT Signals Connectivity table

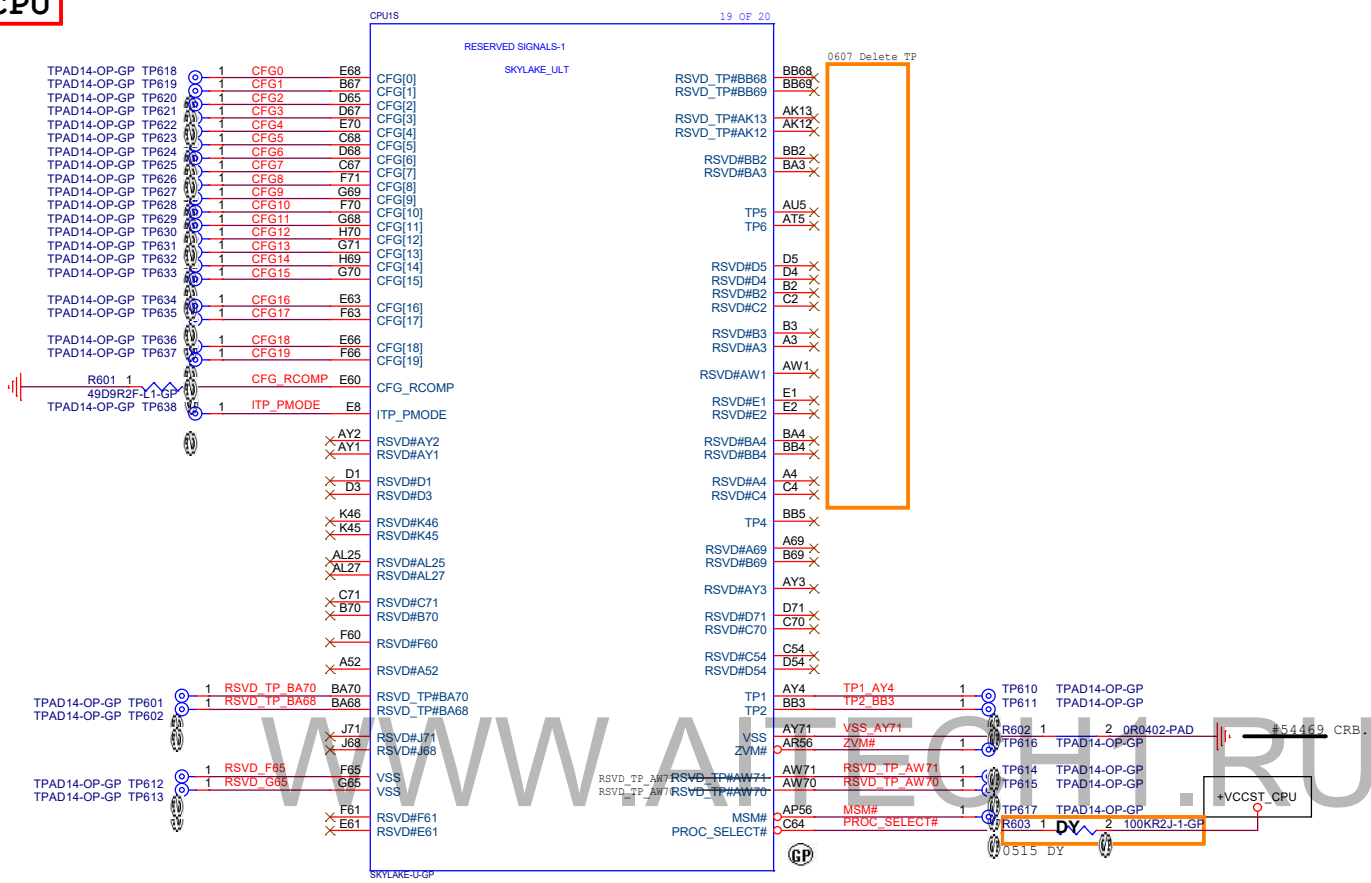
Processor	Memory	Side	Signal	Rule	Notes
SKL-Y	LPDDR3 Memory Down	Processors	DDR0_ODT[0] DR01_ODT[0]	Processor's ODT[0] connected to DRAM's ODT. Topology connection	1,2
			DDR0_ODT[1:0] DR01_ODT[1:0]	Processor's ODT[1] connected to DRAM's ODT. Topology connection. Processor's ODT[1] not connected.	1,2
SKL-U	LPDDR3 Memory Down	Processors	DDR0_ODT[0] DR01_ODT[0]	Processor's ODT[0] connected to DRAM's Rank0 ODT. Processor's ODT[1] connected to DRAM's Rank1 ODT. If Rank1 not used, Processor ODT[1] not connected.	3,4
			DDR0_ODT[1:0] DR01_ODT[1:0]	Processor's ODT[1] connected to DRAM's Rank0 ODT. Processor's ODT[1] connected to DRAM's Rank1 ODT. If Rank1 not used, Processor ODT[1] not connected.	3,4
DDR3L SO-DIMM	Processor	DIMMs	DDR0_ODT[0] DR01_ODT[0]	Processor's ODT[0] connected to DIMM. Processor's ODT[1] connected to DIMM. Processor's ODT[1] not connected.	3,4
			DDR0_ODT[1:0] DR01_ODT[1:0]	Processor's ODT[1] connected to DIMM. Processor's ODT[1] not connected.	3,4
DDR4 Memory Down	Processor	DIMMs	DDR0_ODT[0] DR01_ODT[0]	Processor's ODT[0] connected to DIMM. Processor's ODT[1] connected to DIMM. Processor's ODT[1] not connected.	3,4
			DDR0_ODT[1:0] DR01_ODT[1:0]	Processor's ODT[1] connected to DIMM. Processor's ODT[1] not connected.	3,4
DDR4 SO-DIMM	Processor	DIMMs	DDR0_ODT[0] DR01_ODT[0]	Processor's ODT[0] connected to DIMM. Processor's ODT[1] connected to DIMM. Processor's ODT[1] not connected.	3,4
			DDR0_ODT[1:0] DR01_ODT[1:0]	Processor's ODT[1] connected to DIMM. Processor's ODT[1] not connected.	3,4

Notes:
1. Additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files (CPUV3 - SKL-Y LPDDR3, CPUV4 - SKL-Y LPDDR3).
2. DDR3L ODT input is held high (Active). RET_N is defined by BIOS as high-Z in both cases, when a Rank receives write command RET_N is left by BIOS after power state change. Otherwise ODT is left by BIOS after power state change.
3. These guidelines are related to DDR3L supported Memory down topologies only. 2R x16 DDP single side, 2R x16 DDP dual sided and 2R x8 DDP dual side.
4. NOD (High-Z)

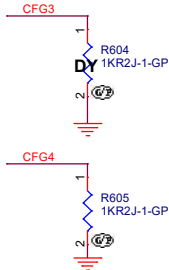


Core Design

Main Func = CPU



PCH strap pin:



[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

(#543016)	
DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port. 1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

CFG TERMINATIONS

20140807 david

#544669 Rev0.52 (CRB)

SKL(#543016) :
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

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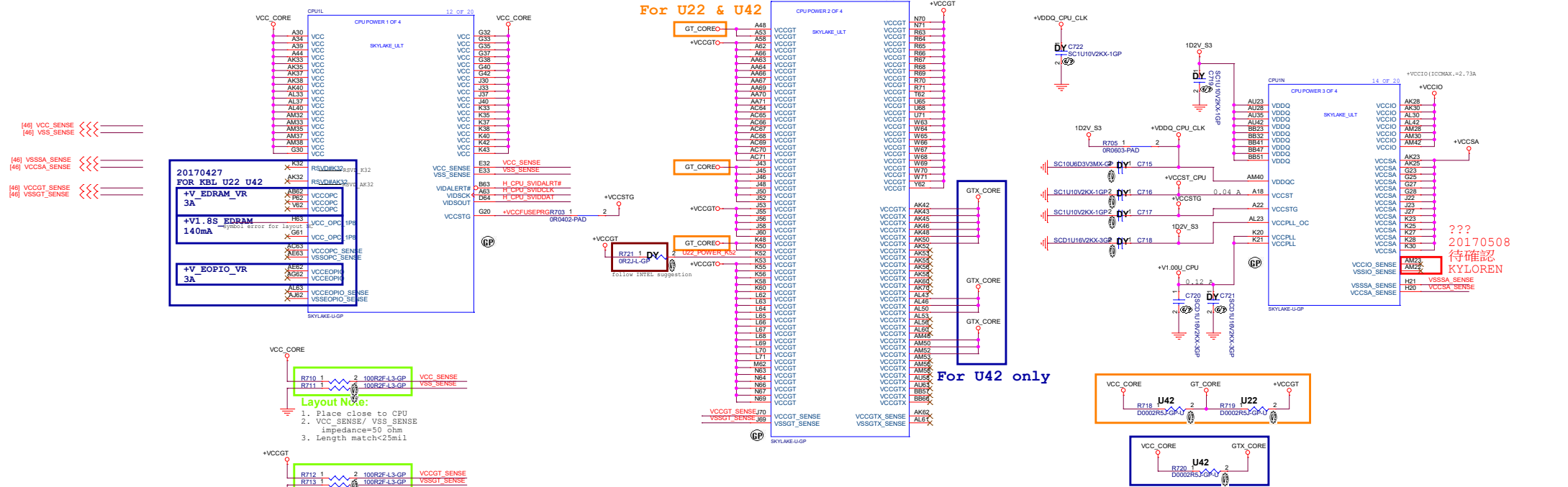
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Size: A3 Document Number: **Vegas SKL/KBL-U** Rev: A00

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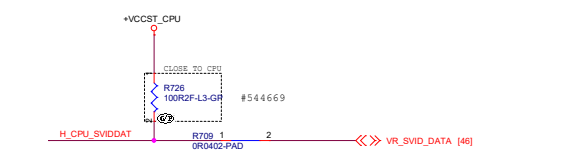
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For U22 & U42



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Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.

SVID DATA



SVID CLOCK

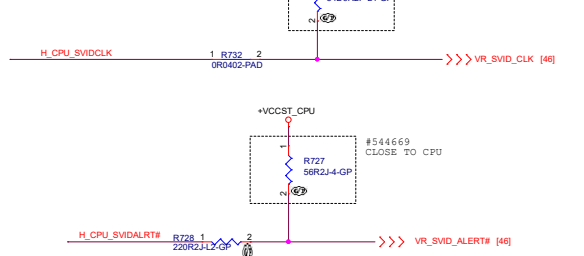
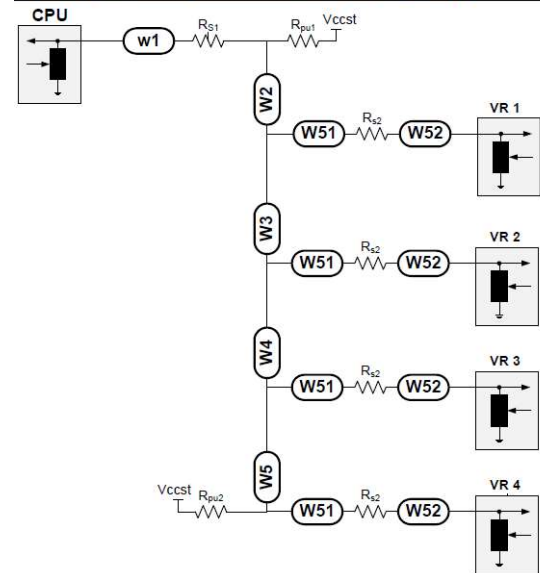


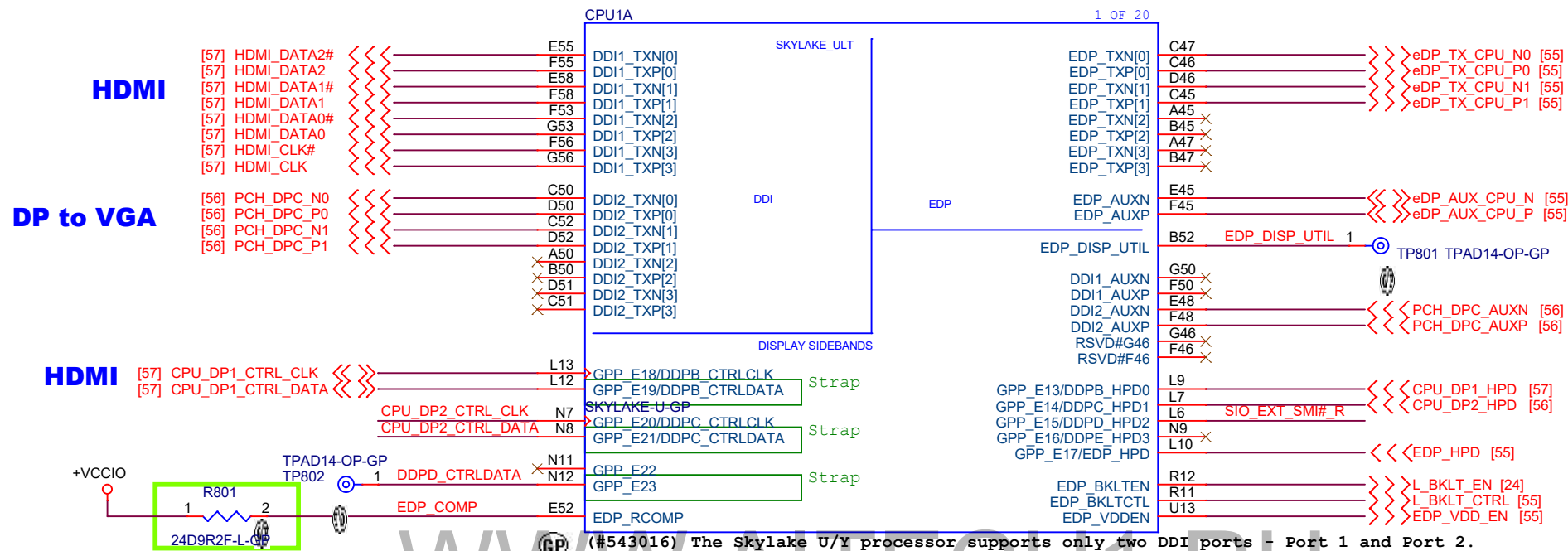
Figure 10-7. Routing Illustration for SVID Topology



SVID_543016:
Table 10-10. SVID Bus Routing Guidelines

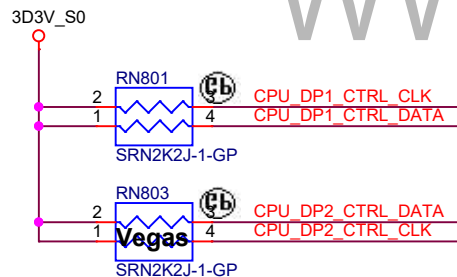
Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R511 [Ω]	R512 [Ω]	R51 [Ω]	R52 [Ω]	VCCGT [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

Main Func = CPU



(#543016) The Skylake U/Y processor supports only two DDI ports - Port 1 and Port 2.

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 $\pm 1\%$ Ω resistor.



(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω $\pm 1\%$	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines


Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k $\pm 5\%$ resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k $\pm 5\%$ resistor	NC

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. ★ 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. ★ 1 = Port C is detected.

These two signals have weak internal pull-down.

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CPU (DISPLAY)
Vegas SKL/KBL-U

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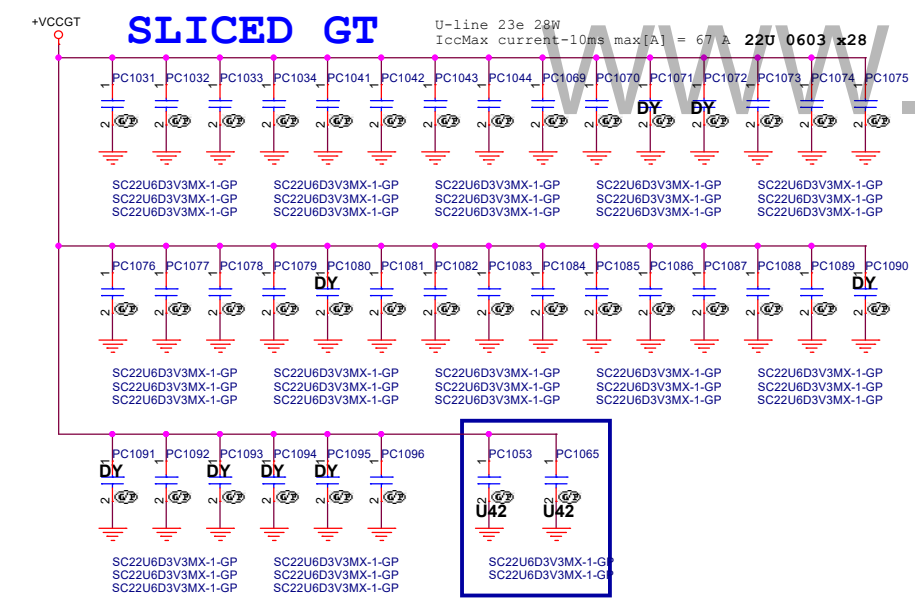
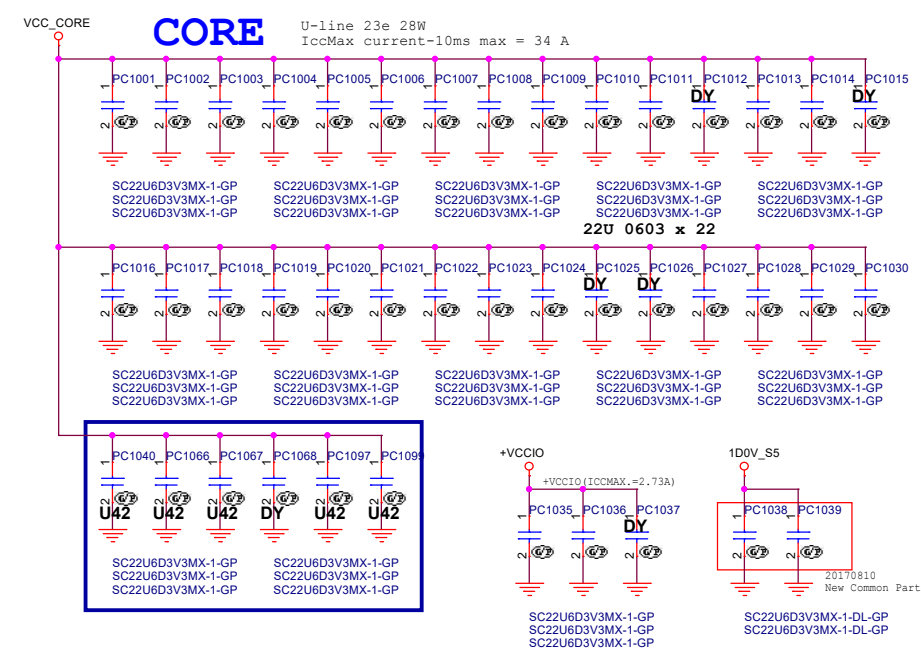
Vegas SKL/KBL-U

Rev
A00

Date: Wednesday, November 08, 2017

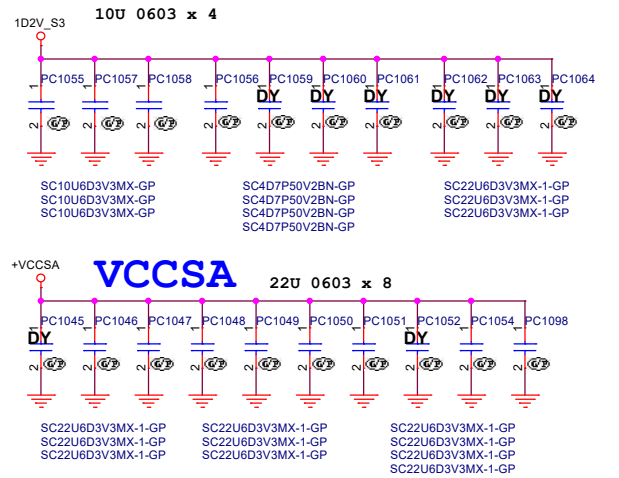
Sheet 9 of 105

Main Func = CPU



KBL-R U42 / KBL U 22 Decoupling Requirements (Sheet 2 of 3)

Domain	Backside cap	Primary side cap	Placement guideline
VCCPLL		1x 1 uF 0402	Place as close to the package as possible.
VCCPLL_DC		1x 1 uF 0201	Do not route VCCPLL_VCCPLL_DC_VCCGT closest adjacent layer over any power net other than ground.
VCCST		1x 1 uF 0402	For VccST: Refer to Figure 48-2 for additional routing details for VccST & VccSTG.



Bulk Decoupling Example (KBL-R U42/KBL U22)

Bulk Decoupling Locations	Example - U 4+2	Example - U 2+2	Notes
Vcc Power Plane at VR output	2x 220 uF (@4.5mO ESR)	1x 220 uF (@4.5mO ESR)	Placed at primary side near to VR output
VccGT Power Plane at VR output	2x 220 uF (@4.5mO ESR)		Placed at primary side near to VR output
VDDQ Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
VCCIO Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
VCCPL Power Plane at V1P0A VR output	1x 0.1uF 0402		Placed at primary side near to VR output

Notes:
1. These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

KBL-R U42 / KBL U 22 Decoupling Requirements (Sheet 1of 3)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc	7x 10 uF 0402		Place on secondary side, underneath the package
	31x 1 uF 0402 or 0201		Refer to diagram in Note 4 below for placement recommendation of 0402 caps Refer to diagram in Note 5 below for placement recommendation of 0201 caps
		9x 22 uF 0603	Place as close to the package as possible
		8x 47 uF 0805 (6.3V) ¹	
		8x 10 uF 0402	
Vcc/VccGT	5x 1 uF 0402 or 0201		Place as close to the package as possible
VccGT	12x 10 uF 0402		Place on secondary side, underneath the package
	14x 1 uF 0402 or 0201		
VccSA		7x 22 uF 0603	Place as close to the package as possible
		3x 47 uF 0805 (6.3V) ¹	
	7x 10 uF 0402		Place on secondary side, underneath the package
	7x 1 uF 0402 or 0201		
VccIO		6x 10 uF 0402	Place as close to the package as possible
		4x 1 uF 0402	Place as close to the package as possible
VDDQ		4x 10 uF 0402	Place as close to the package as possible
		3 x 22 uF 0603	Place as close to the package as possible
VDDQC		1 x 10 uF 0402	Preferred to place the 0402 10uF cap on the secondary under the package shadow near VDDQC pin and short to VDDQ rail under with a shape. Alternatively, if the 0402 cap cannot be placed on the backside, follow the example showed in Figure 48-3. The 0402 cap to VDDQC BGA routing should not exceed 48mm (Rdc). RVP design uses trace L=450mil, W=8mil between BGA and cap. Additional trace routing implemented in RVP design was not required.

Note: Refer to latest revision of KBL- RU PDG for final specifications

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Size A3 Document Number **Vegas SKL/KBL-U** Rev **A00**

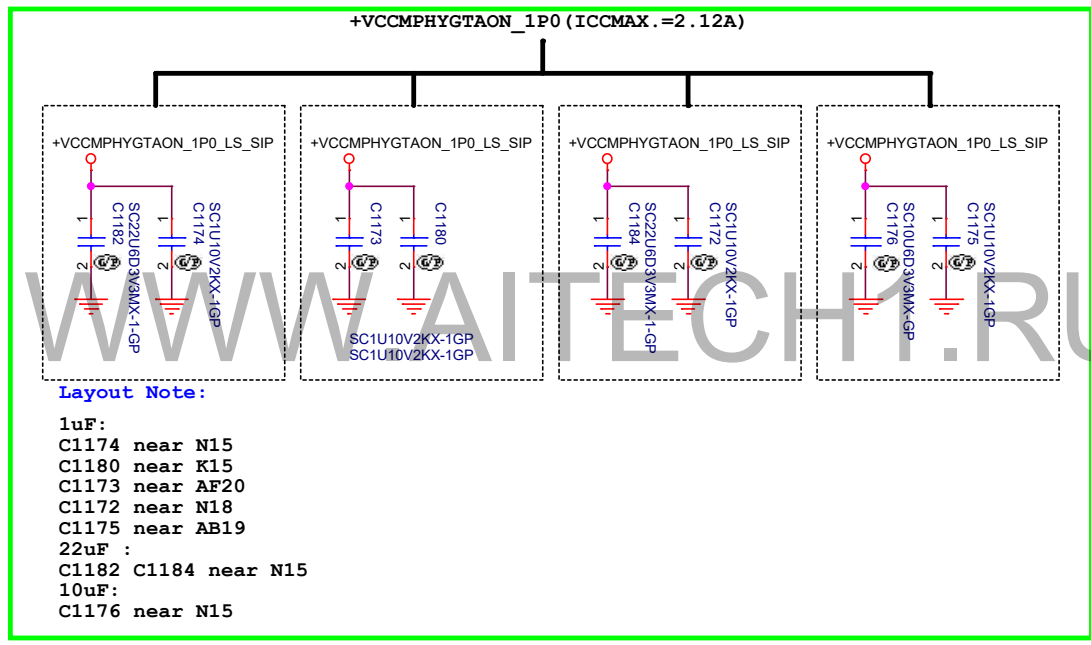
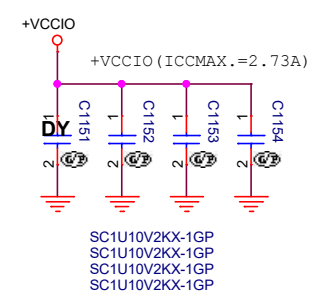
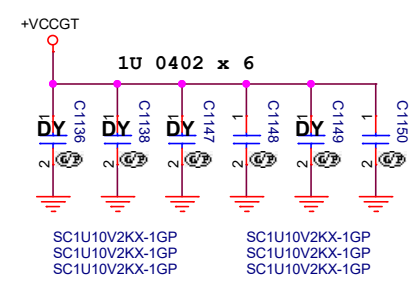
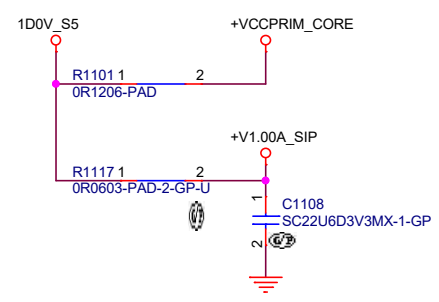
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Main Func = CPU

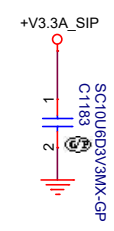
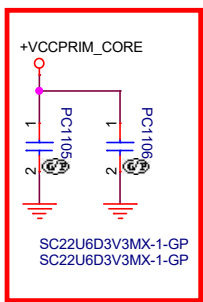
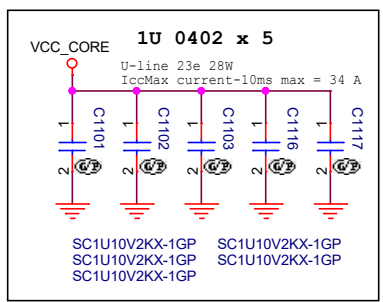
PCH DERIVED RAILS

UNSLICED GT


VCCIO



Layout Note:
1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15



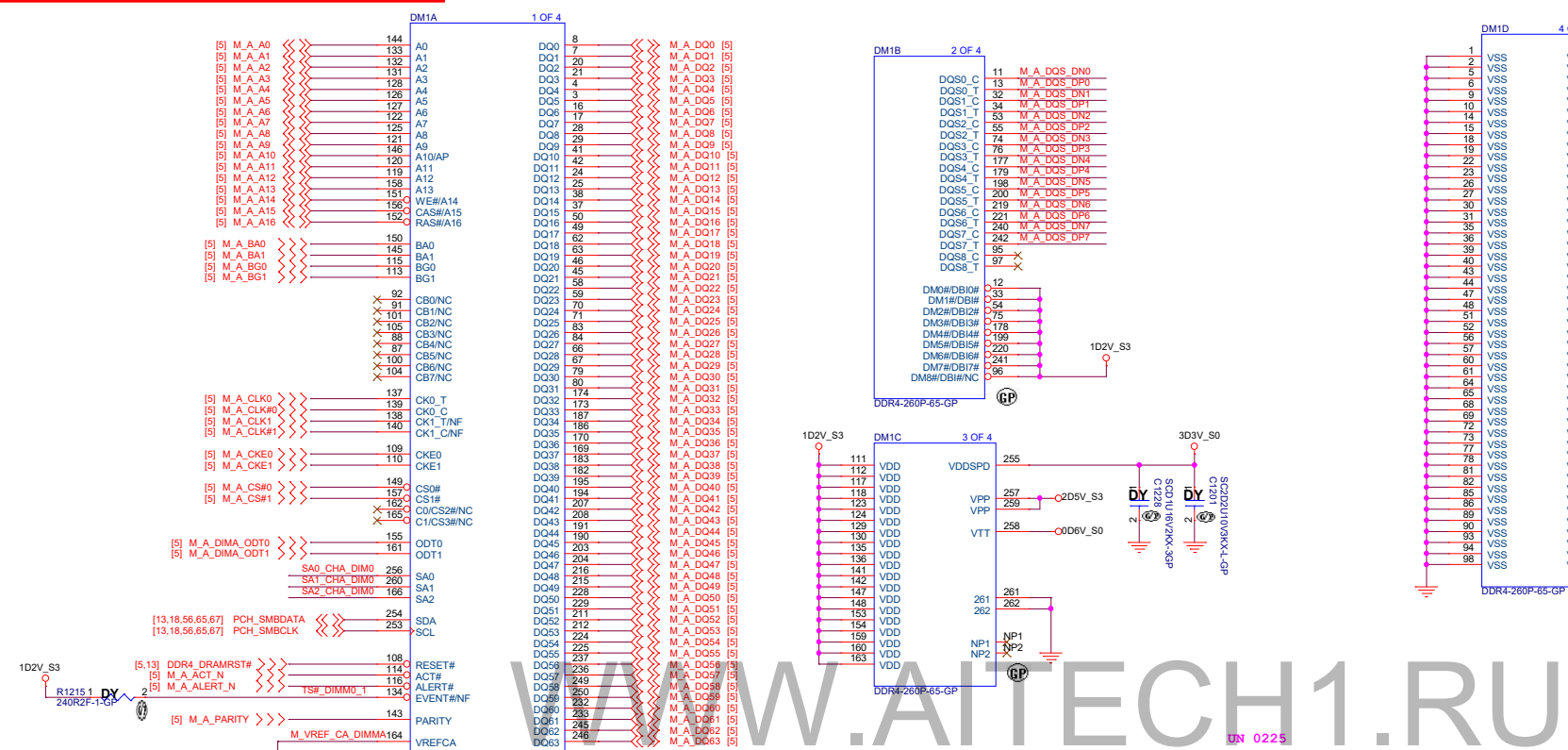
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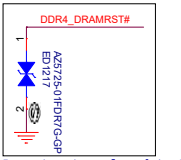
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Main Func = DDR4 SODIMM

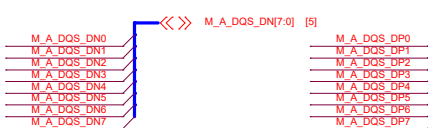
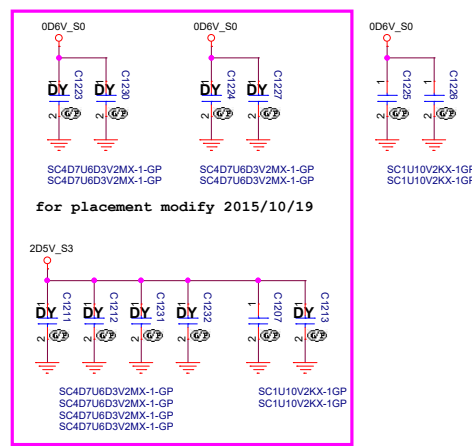
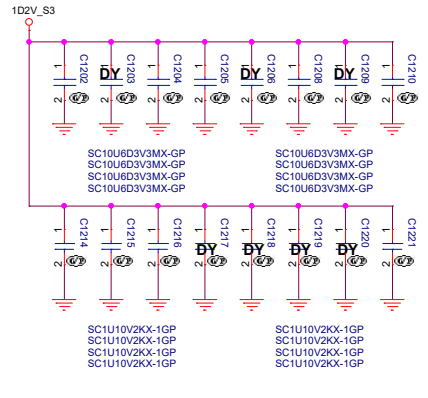
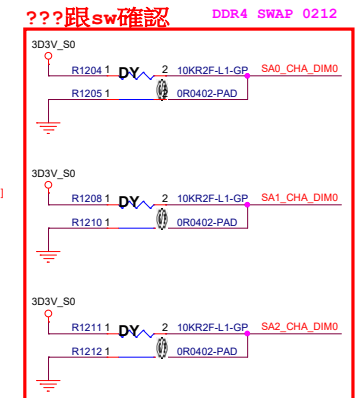
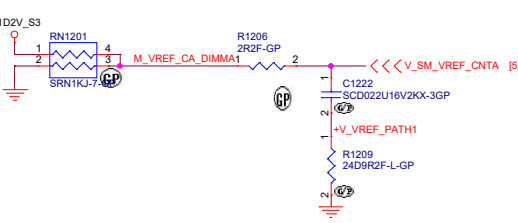


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Layout note: closed to Dimm



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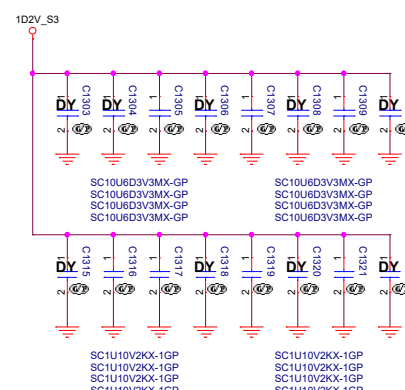
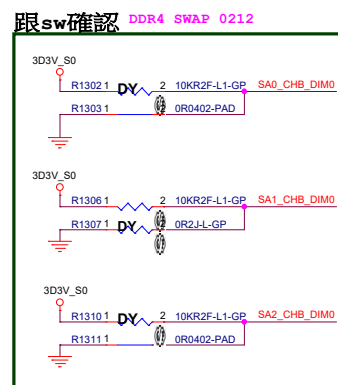
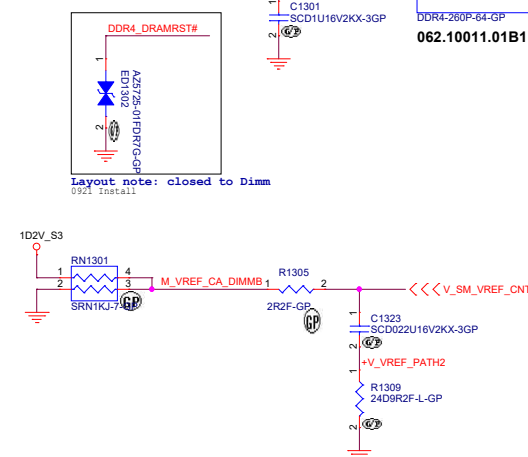
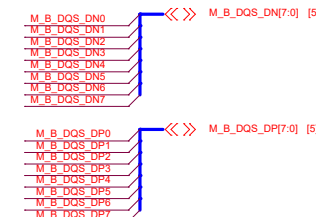
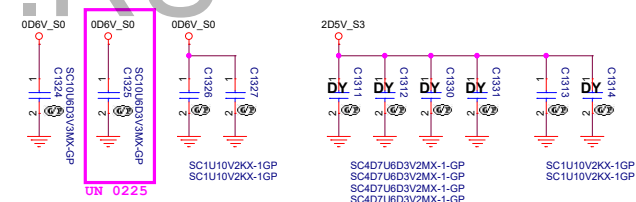
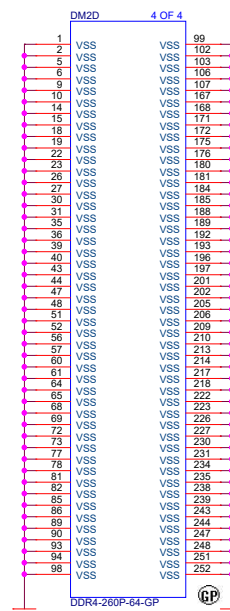
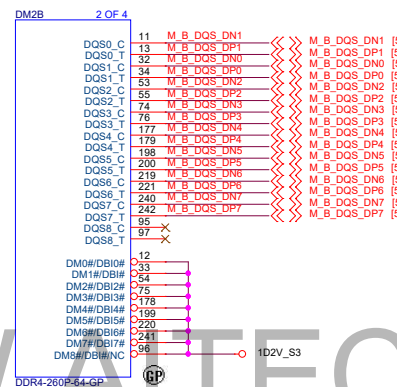
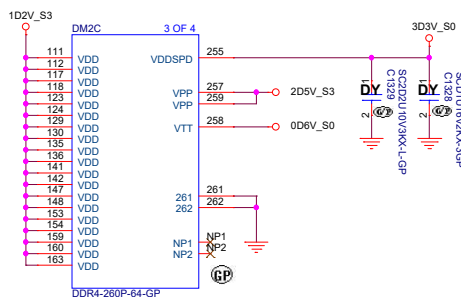
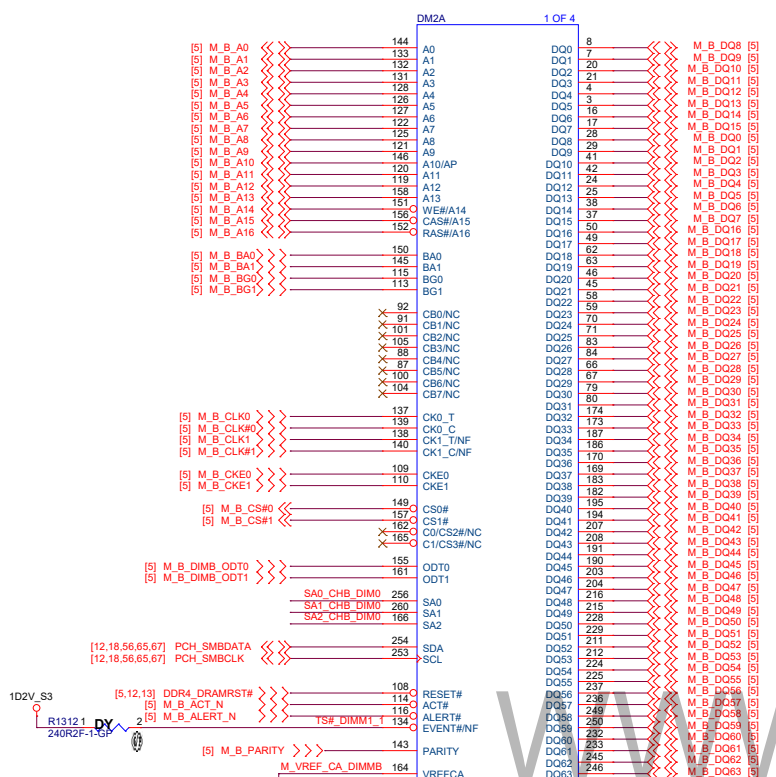
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Date: Wednesday, November 08, 2017 12 of 106

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Main Func = PCH

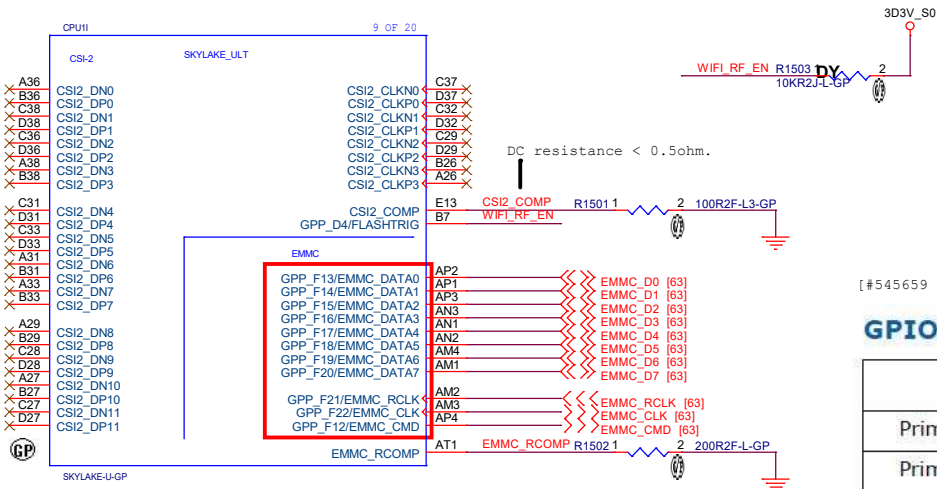


Table 8-1. Switchable Graphics GPIO Requirements

GPIO	Usage
DGPU_PWR_EN#	BIOS drives to turn on/off the discrete graphics power.
DGPU_PWROK	dGPU voltage regulator drives to indicate power status to the PCH. It enables clocks to dGPU.
DGPU_HOLD_RST#	Discrete Graphics Enable signal. BIOS controls and a PCH GPIO drives. It gates Platform Reset to enable Reset for the dGPU.
DGPU_PRSENT#	Used only by the CRB or if Graphic Cards requiring AC caps on the motherboard or add-in card is supported on the platform to indicate that a card is present.

[#545659 Rev0.7]

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

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FILE

CPU (CS-2/EMMC)

Size A3

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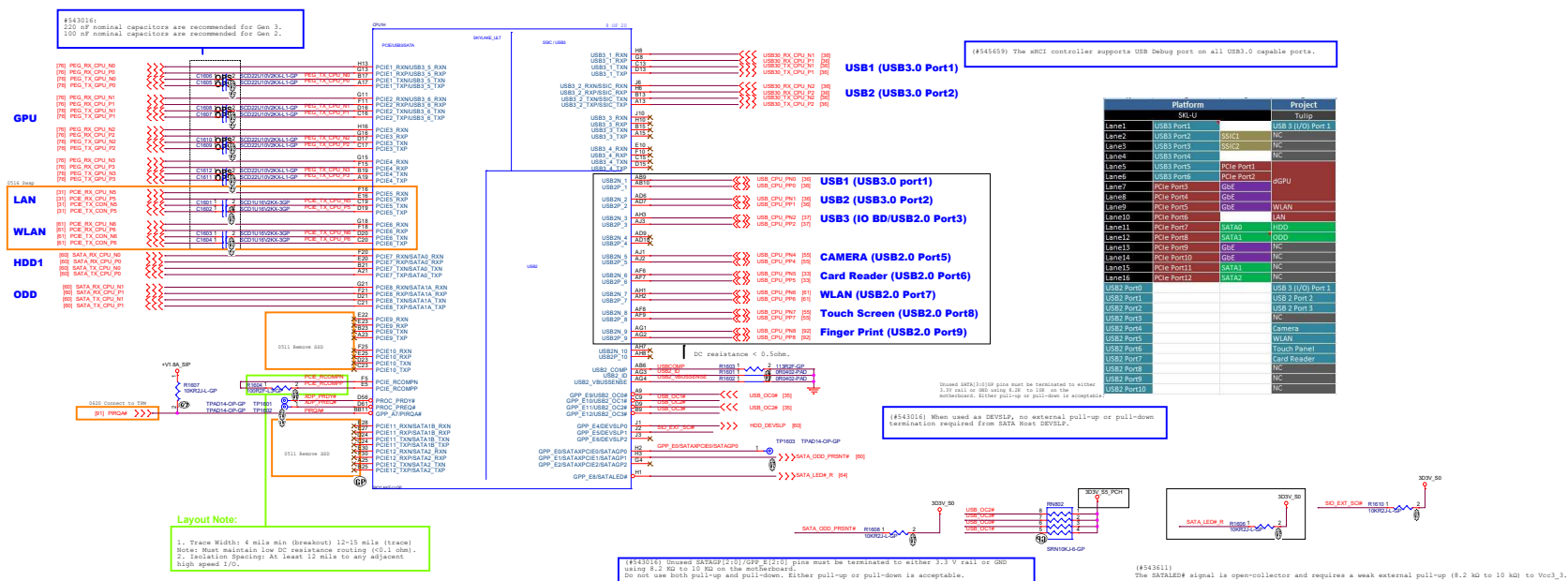
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PCIe Table

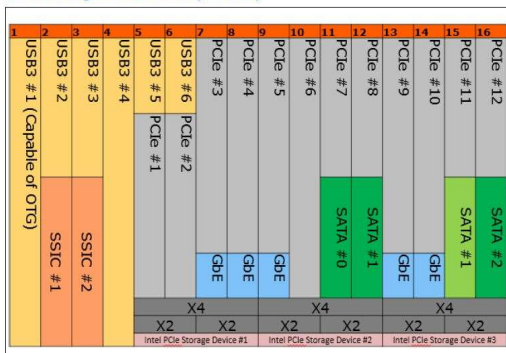
Port	Device	Share SIOB
0	N/A	USB3_0_3
1	N/A	USB3_0_4
2	WLAN	
3	LAN	
4	LAN	
5 (LO-L3)	GPU	
6 (L3)	HDD	SATA0
6 (L2)	ODD	SATA1
6 (LO-L1)	N/A	

USB 2.0 Table

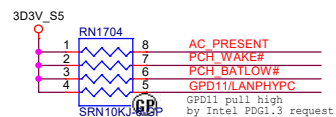
Pair	Device
0	USB3.0 Port1
1	USB3.0 Port2
2	USB2.0 Port3 (IOBD)
3	Finger Print
4	CAMERA
5	Card Reader
6	Touch Panel
7	WLAN

#545659 (SKL_PCH_U_Y_R0 Rev0.7)

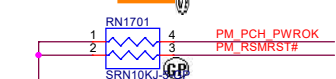
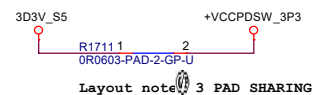
Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)



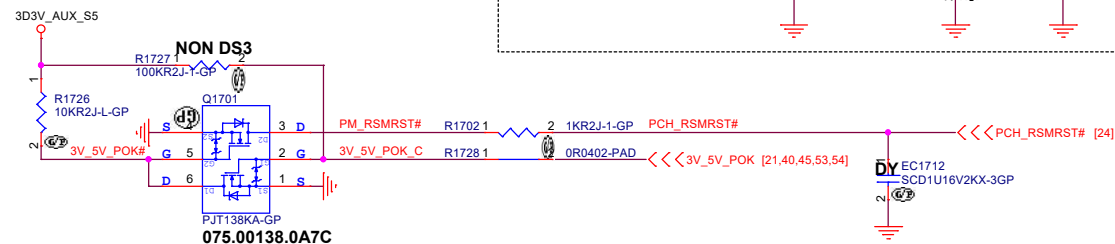
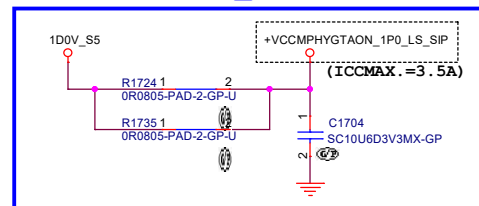
Main Func = PCH



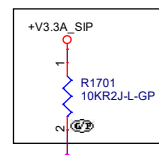
BATLOW#:
Pull-up required even if not implemented.



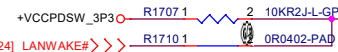
+VCCMPHYGTAON 1P0



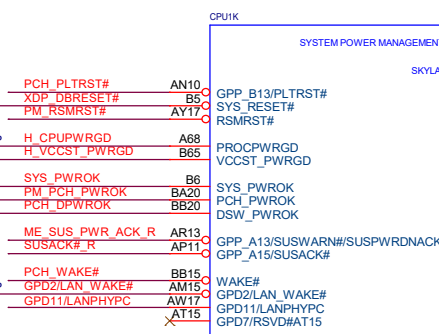
```
[24] SYS_PWROK      >>> _____
[24.26.79] RESET OUT# >>> _____
```



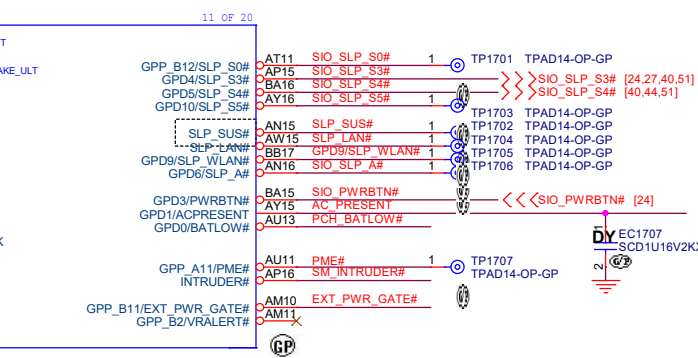
DY for OBFF disable



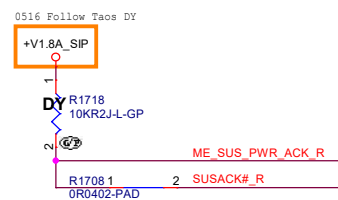
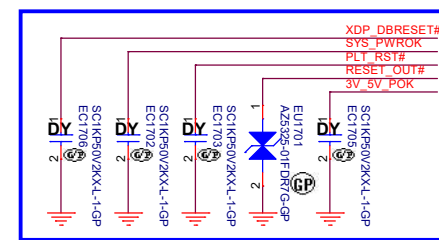
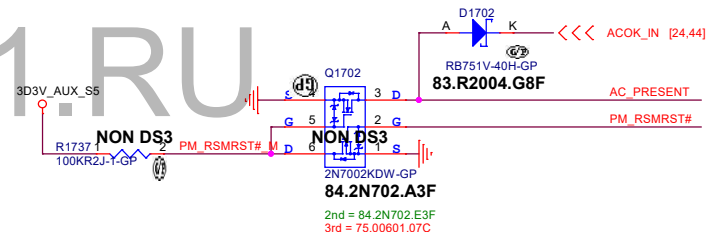
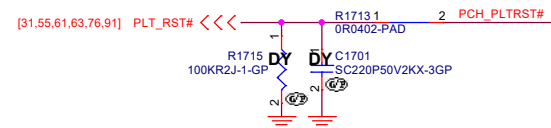
(PDG#543016)
WAKE#: Ensure that WAKE# signal Trise (Maximum) is <100 ns



SKYLAKE-U-GP
071.SKYLA.000U

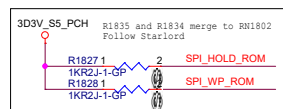


```
[#543016 Rev0.7]
EXT_PWR_GATE#: Due to a bug on A0, a temporary pull-up resistor will be required to overcome the internal 20k
pull-down that is active during the early portion of the power up sequence
```



Main Func = PCH

PCH strap pin:



0511 Follow KY15.



eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC Is selected for EC. 1 = eSPI Is selected for EC.
This signal has a weak internal pull-down.	

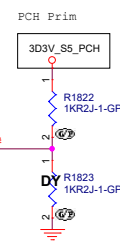
This signal has a weak internal pull-down.

This signal has a weak internal pull-down.

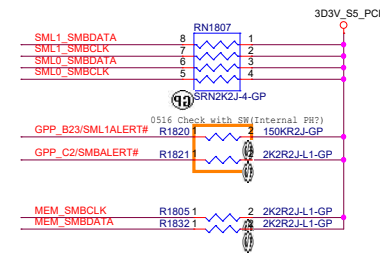
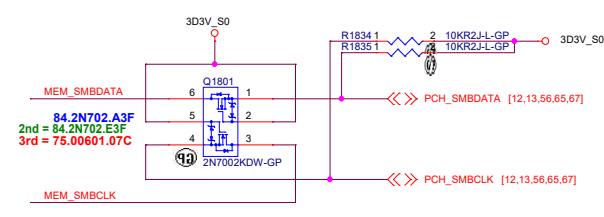
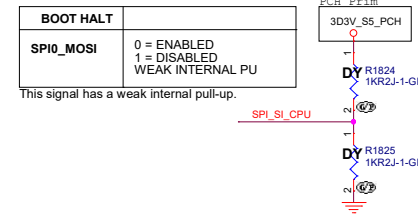
This signal has a weak internal pull-down.

Table 3: Platform Supported Pin Strap Settings for LPC / eSPI / SPI Flash

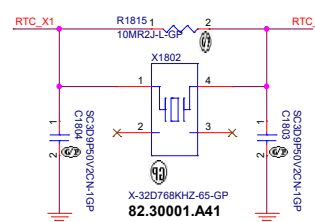
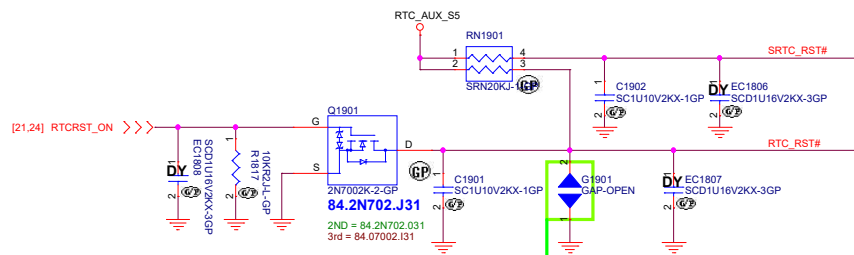
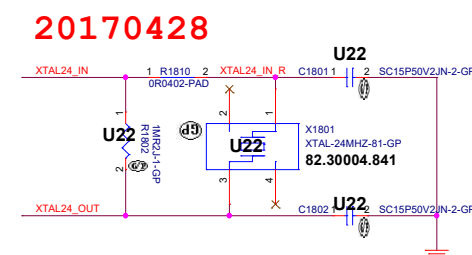
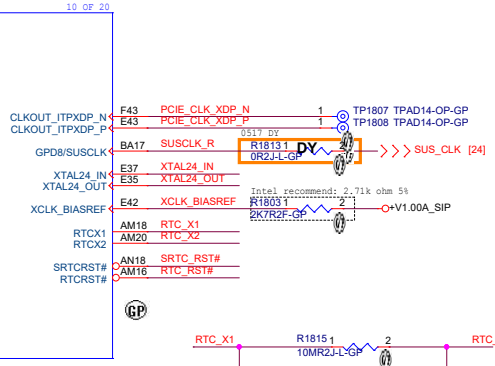
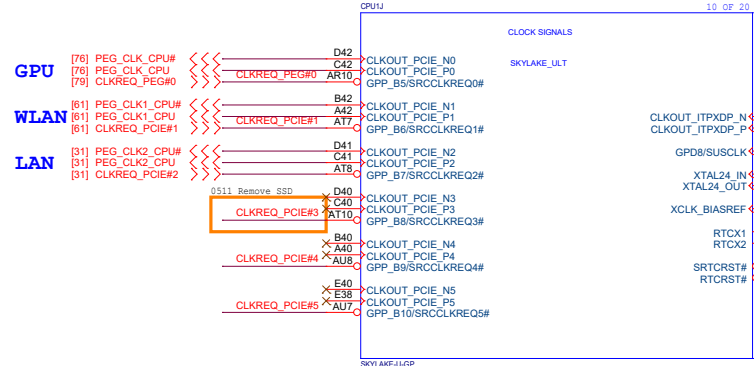
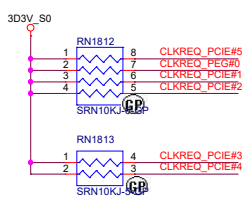
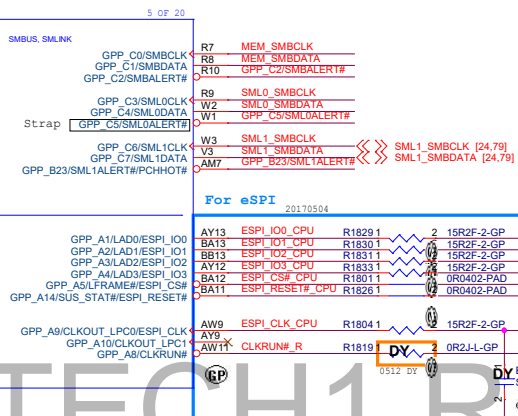
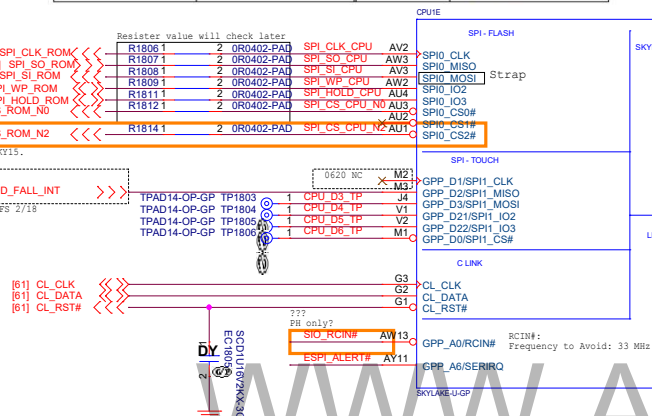
ESPI Enable Strap (ESPI_EN) Value (0: LPC, 1: eSPI)	Boot BIOS Strap (BBS) Value (0: SPI, 1: LPC/eSPI)	EC Connection	Boot (BIOS) Flash Connection (Section 3.1.4)
0	0	LPC	SPI
0	1	LPC	LPC
1	0	eSPI	SPI
1	1	eSPI	eSPI (to EC over eSPI Peripheral Channel) (refer to Section 3.1.4 for details)



PCH strap pin:



eSPI



(#514849)
Layout: Place at the open door area.

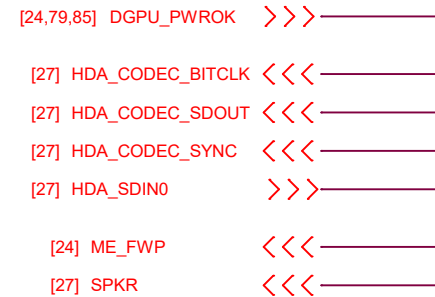
Main Func = PCH

PCH strap pin:

Flash Descriptor Security Override/ Intel ME Debug Mode

HDA_SDOUT	Low = Default High = Enable *
-----------	----------------------------------

The internal pull-down is disabled after PLTRST# deasserts

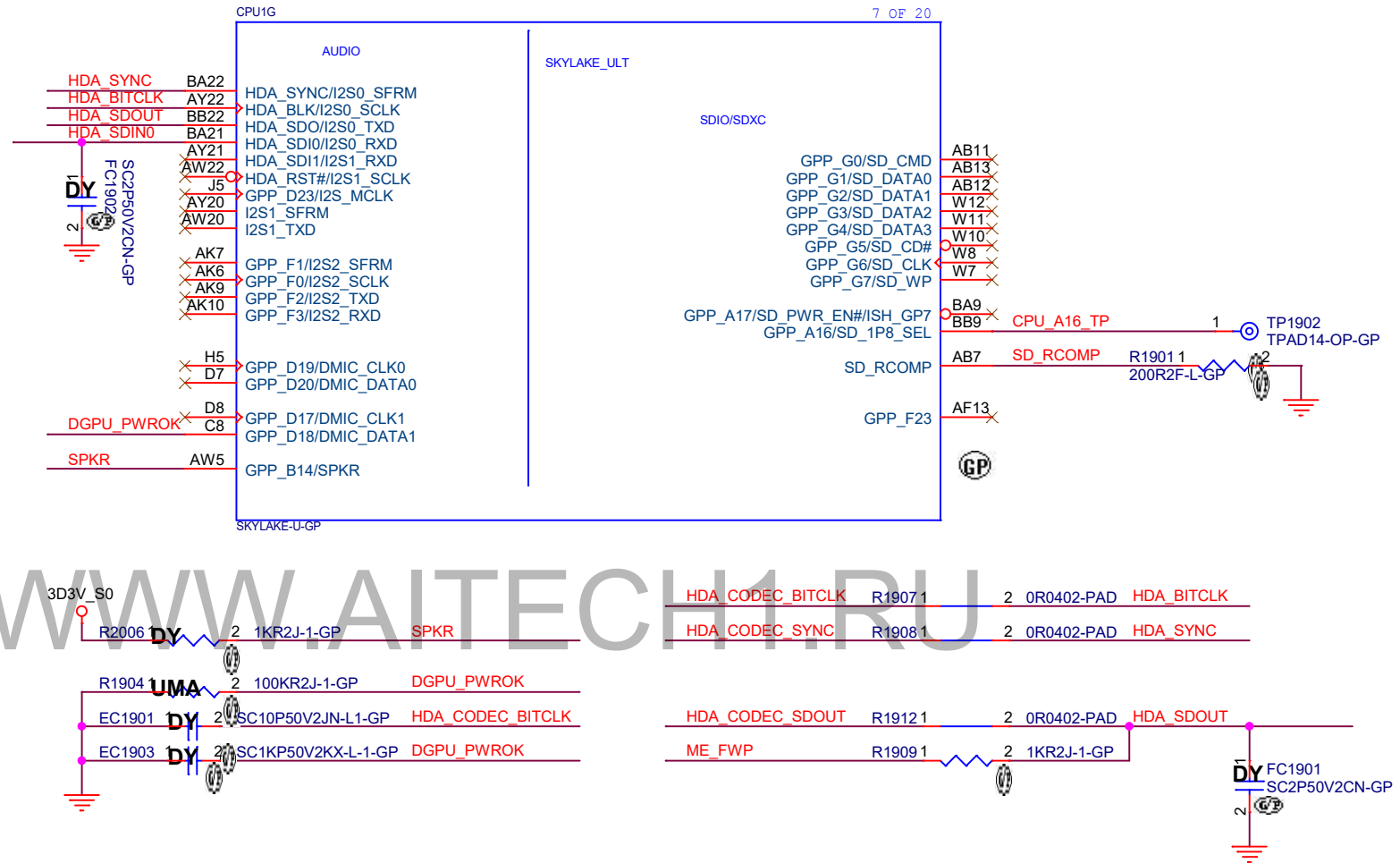


PCH strap pin:

NO REBOOT

HDA_SPKR	<p>* Low = Enable (Default) High = Disable</p>
-----------------	---

The internal pull-down is disabled after PLTRST# deasserts



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Title	
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CPU (AUDIO/SDIO/SDXC)

Size	A4
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Document Number

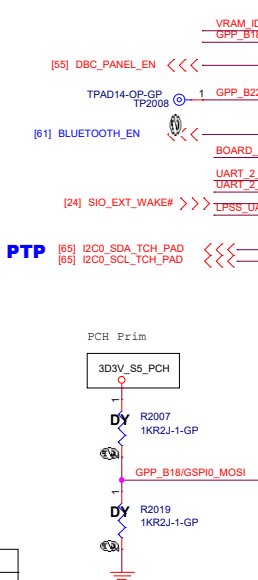
Vegas SKL/KBL-U

Rev
400

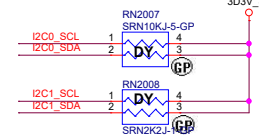
Date: Wednesday, November 08, 2017

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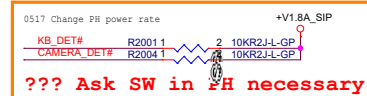
```
[68] UART_2_CRXD_DTXD <<< _____
[68] UART_2_CTXD_DRXD >>> _____
```



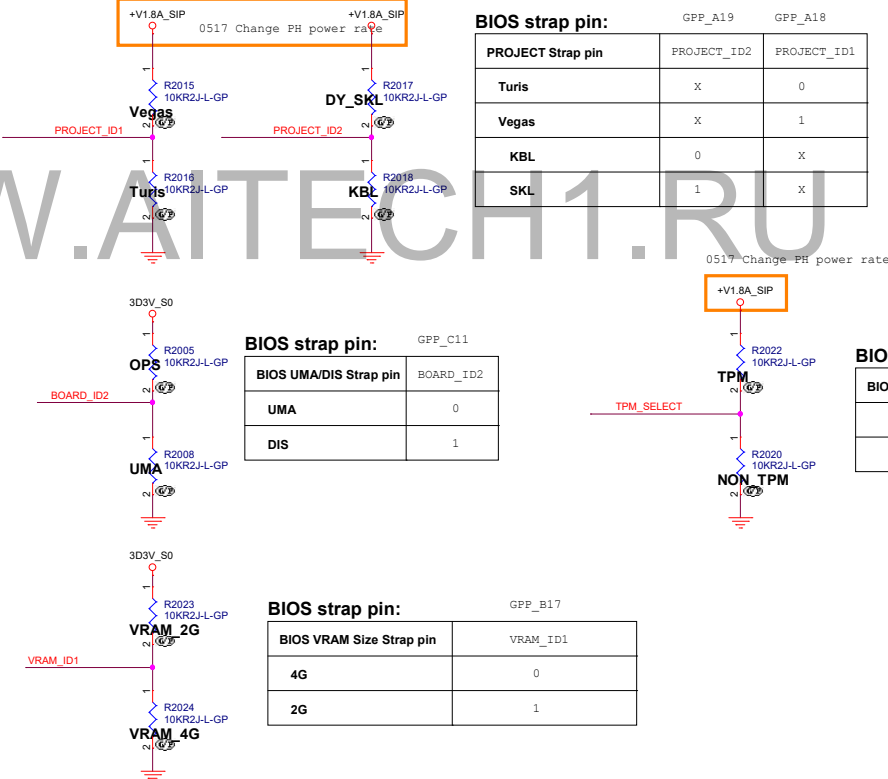
No Reboot	Sampled at rising edge of PCH_PWROK
GSPiO_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.



(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

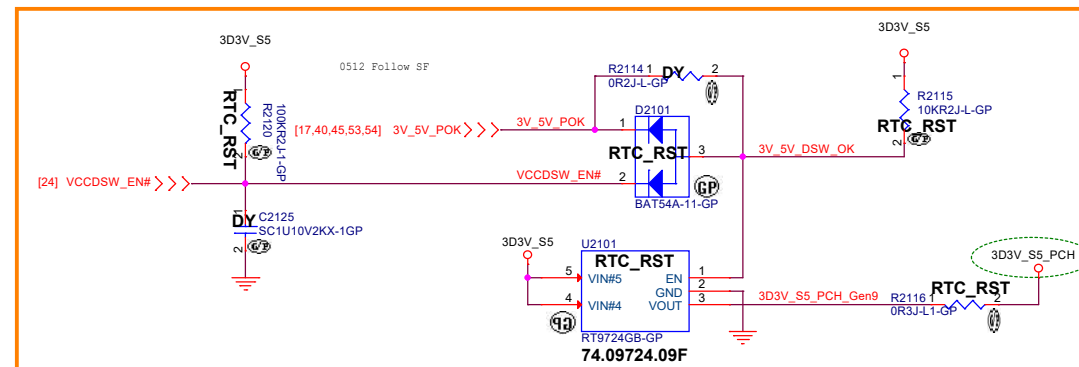
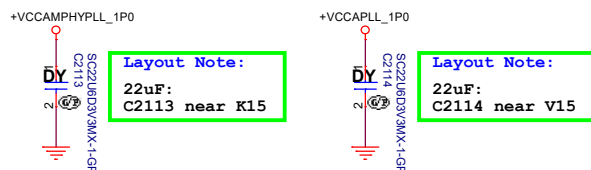
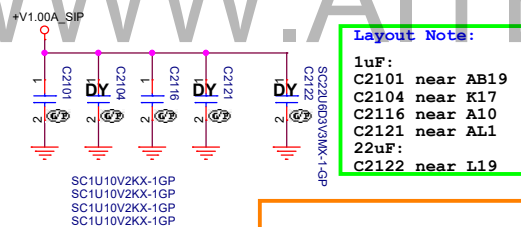
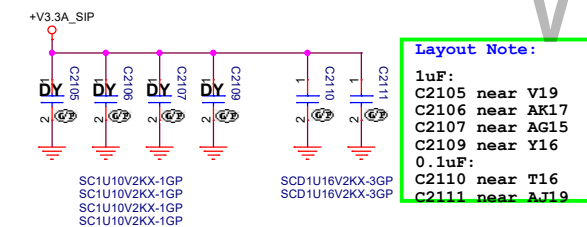
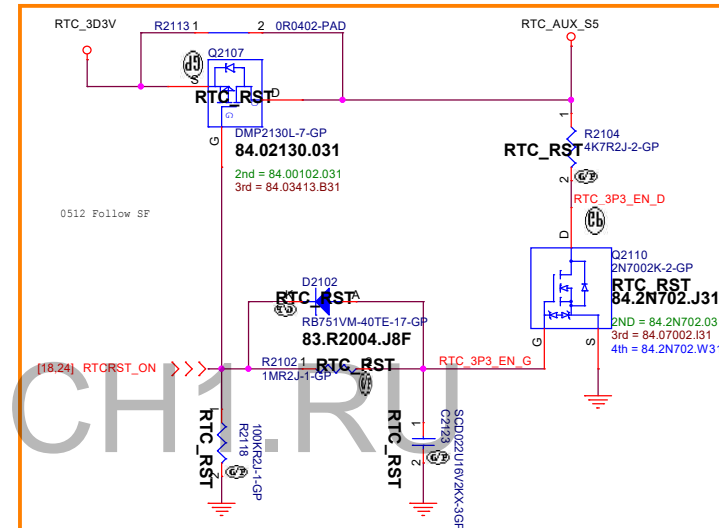
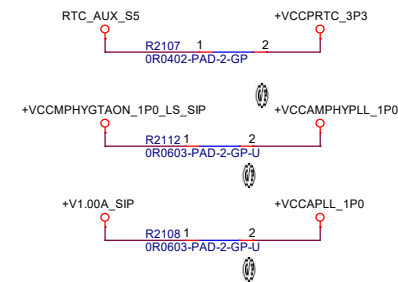
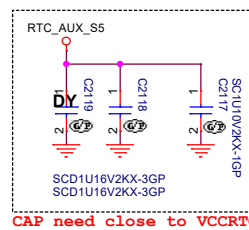
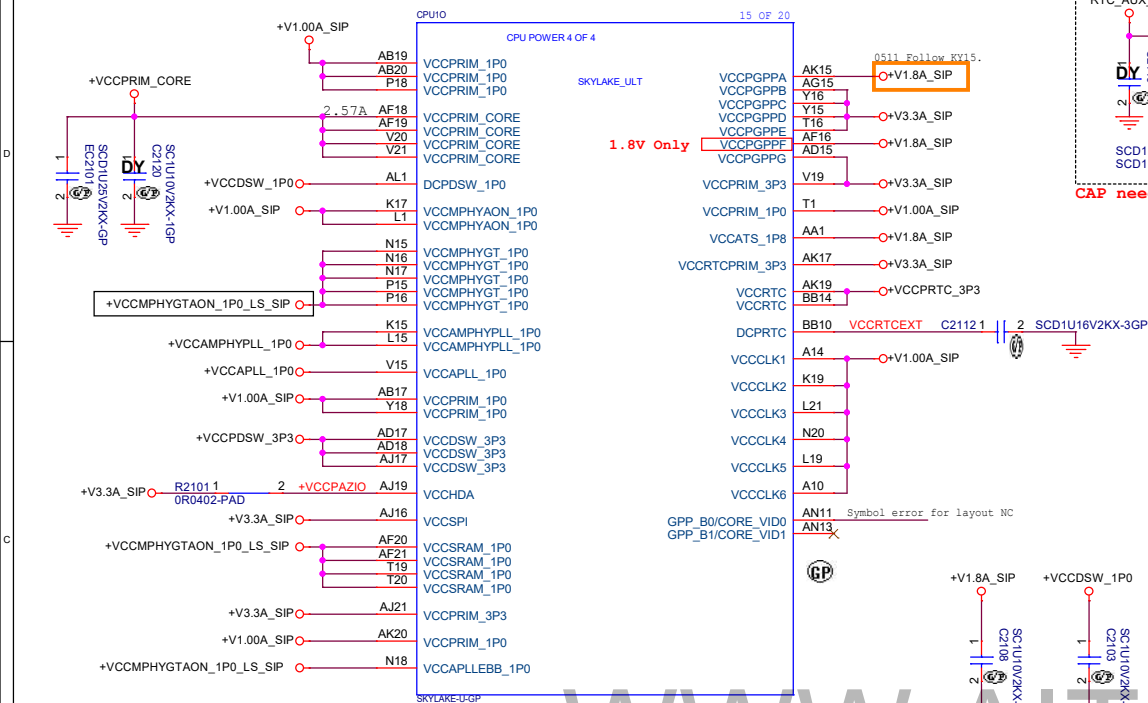


BIOS strap pin:		GFP_A19	GFP_A18
PROJECT Strap pin	PROJECT_ID2	PROJECT_ID1	
Turis	X	0	
Vegas	X	1	
KBL	0	X	
SKL	1	X	



BIOS strap pin: GPP_A22	
BIOS UMA/DIS Strap pin	TPM_SELECT
TPM	1
NON_TPM	0

Main Func = PCH



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Title

CPU (POWER1)Size
A

Document Number

Vegas SKL/KBL-U

Rev
A00

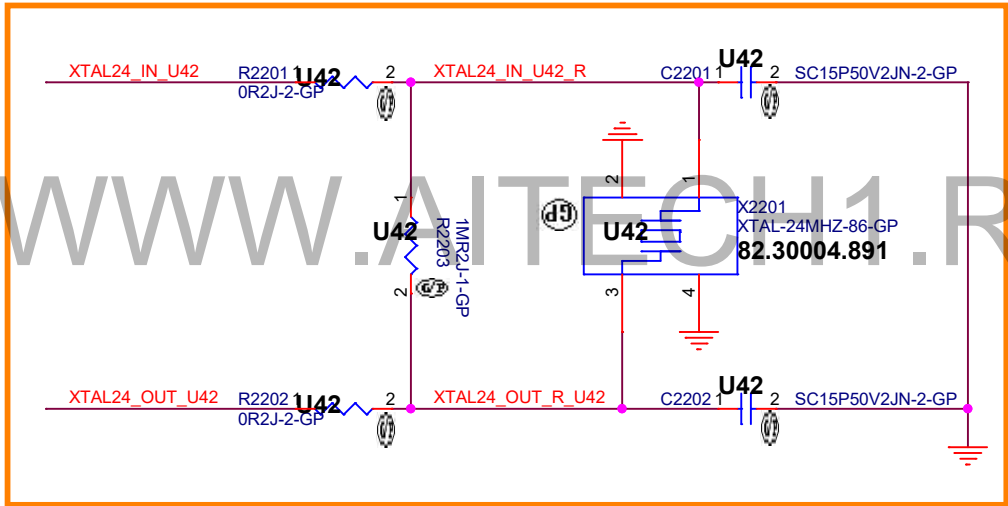
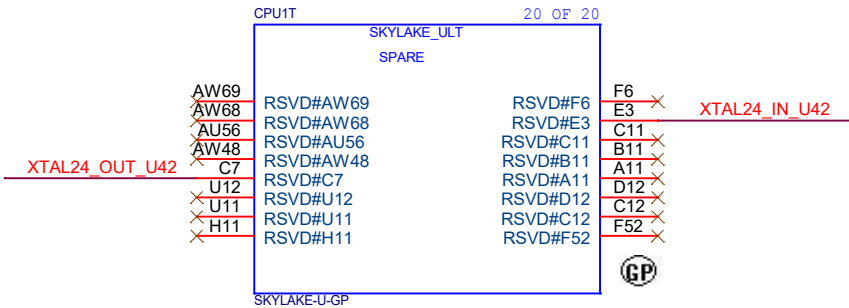
Date: Wednesday, November 08, 2017

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Date: Wednesday, November 08, 2017 Sheet: 21 of 105

Main Func = PCH

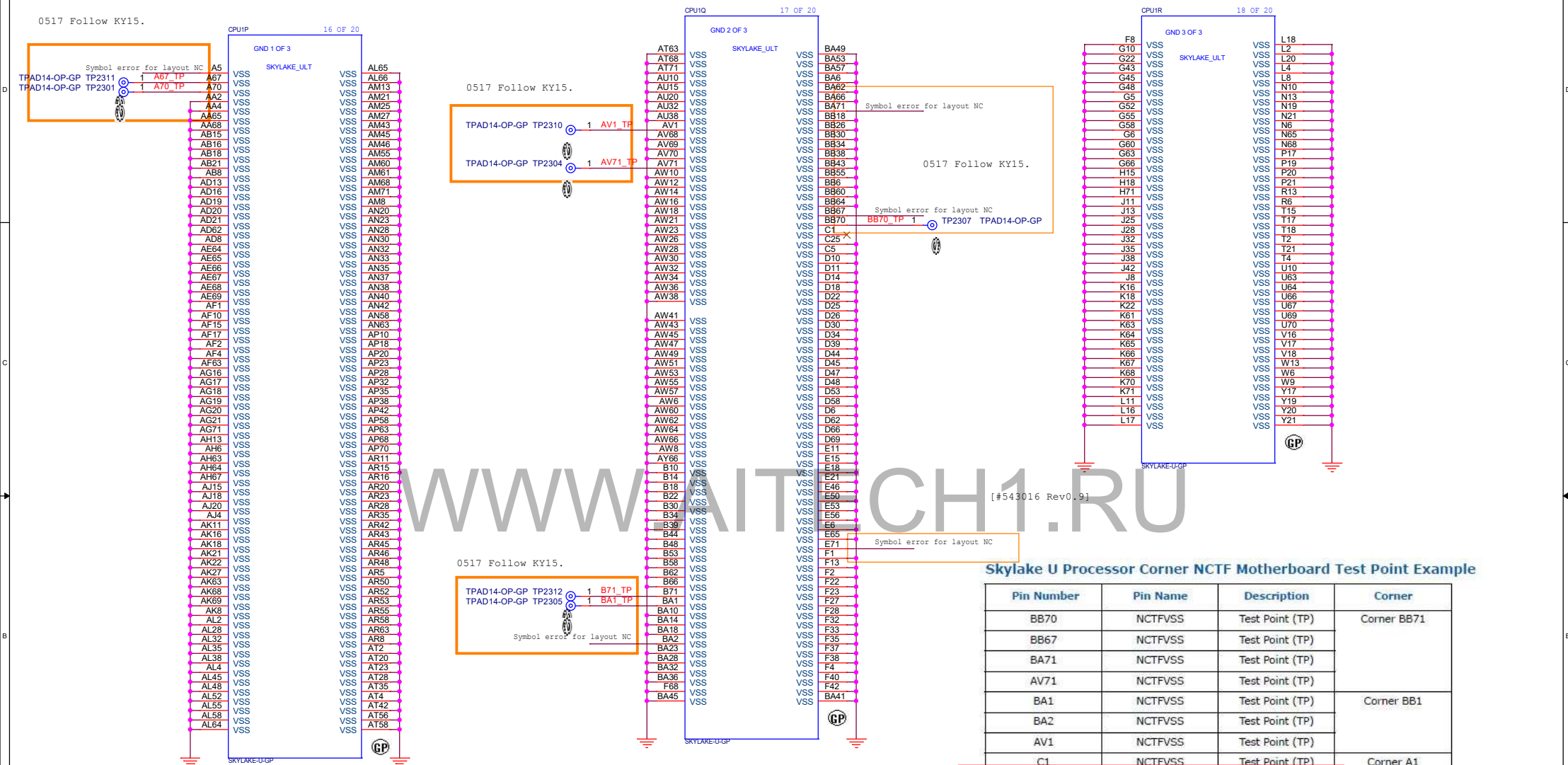
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Title CPU_(RSVD)			
Size A4	Document Number Vegas SKL/KBL-U		Rev A00
Date: Wednesday, November 08, 2017		Sheet 22 of 105	

Main Func = PCH



Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	
A5	NCTFVSS	Test Point (TP)	Corner A1
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

<Core Design>



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	Title
--	-------

CPU (VSS)

Size
A3

Document Number

Vegas SKL/KBL-U

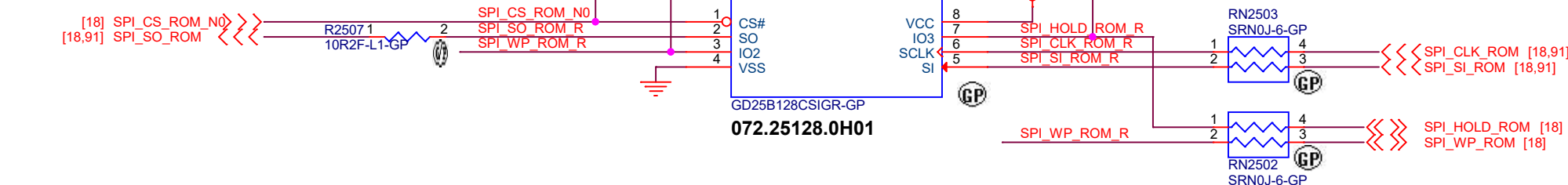
Rev
A00

Date: Wednesday, November 08, 2017

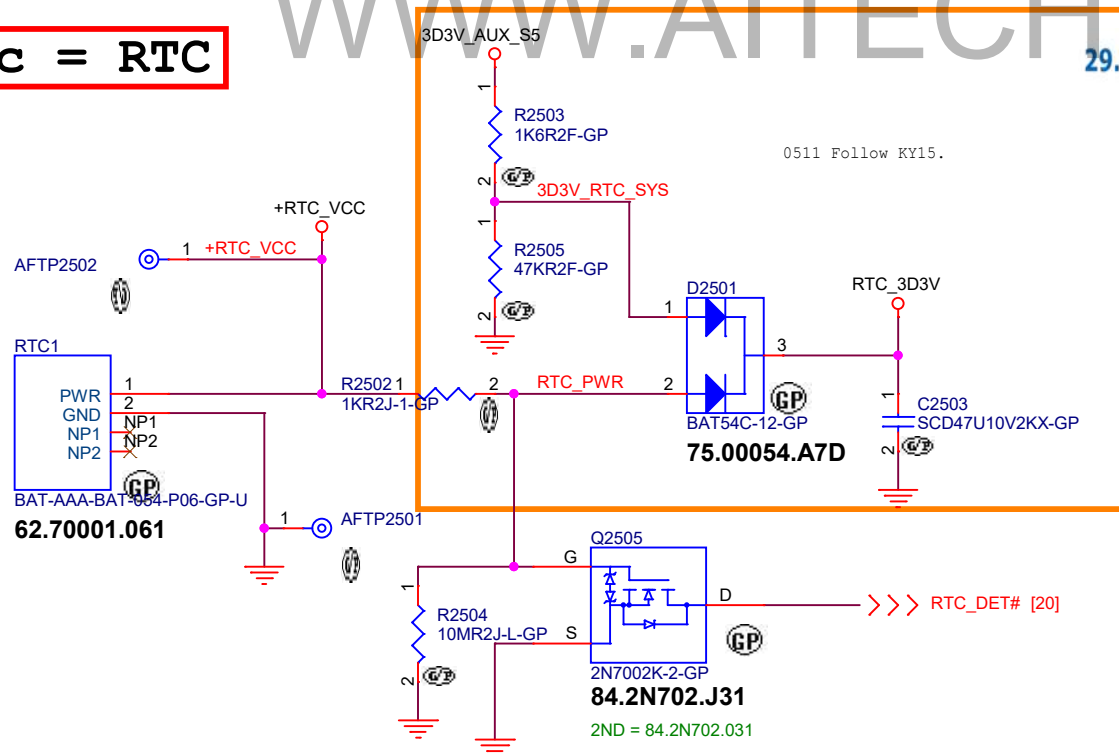
Sheet 23 of 105

Date: Wednesday, November 08, 2017 Sheet 23 of 105

Main Func = RTC



29.2.1 VCCRTC External Circuit



On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.

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Title

Flash/RTC

Size
A4

Document Number

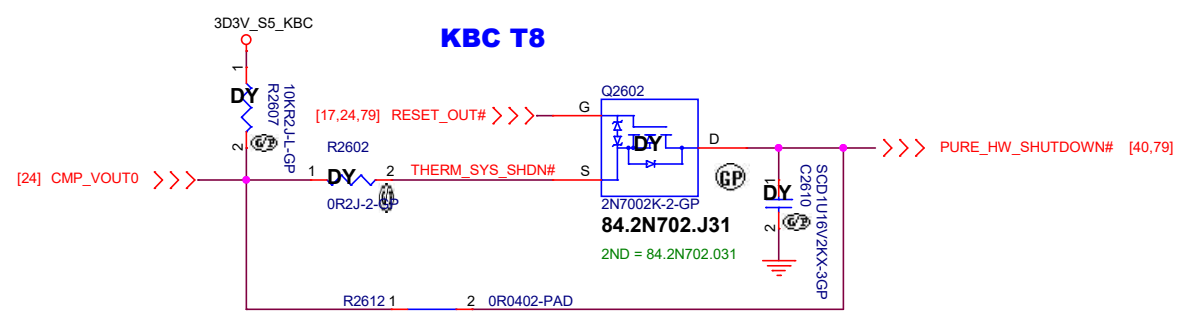
Turis/Vegas KBL-R

Rev
400

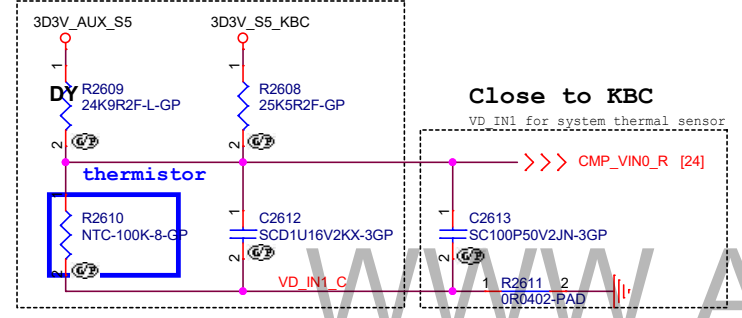
Date: Wednesday, November 08, 2017

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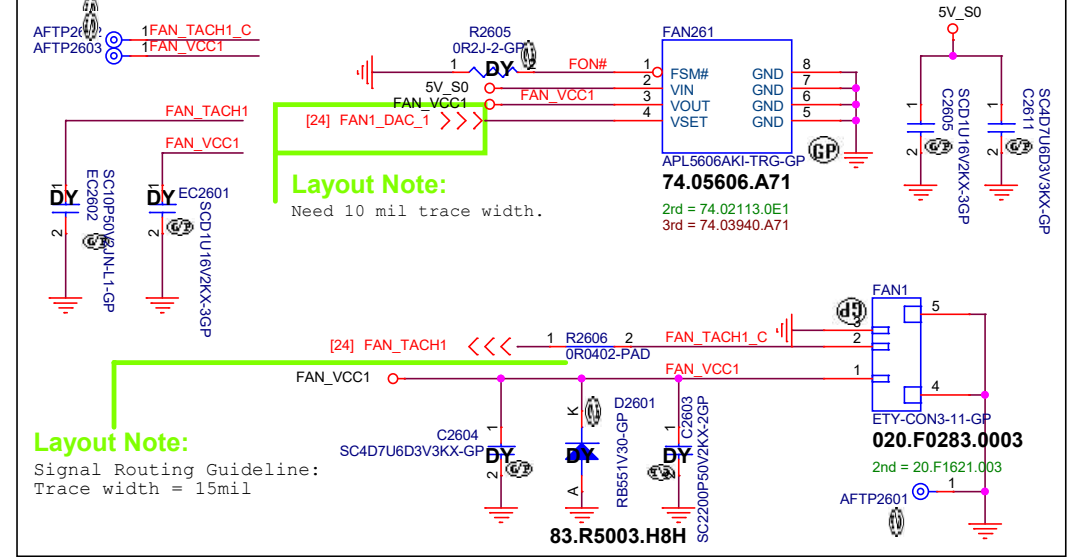
Main Func = Thermal Sensor



Close to Thermal sensor



Fan controller1



Layout Note:
Signal Routing Guideline:
Trace width = 15mil

Layout Note:
Need 10 mil trace width.


change the fan define & connect P/N 020.F0283.0003 by Andy 1/27

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
THERMAL NCT7718W/Fan			
Title	Document Number	Rev	A00
Size	Custom	Turis/Vegas KBL-R	
Date:	Wednesday, November 08, 2017	Sheet	26 of 105

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WWW.AITECH1.RU

<Core Design>

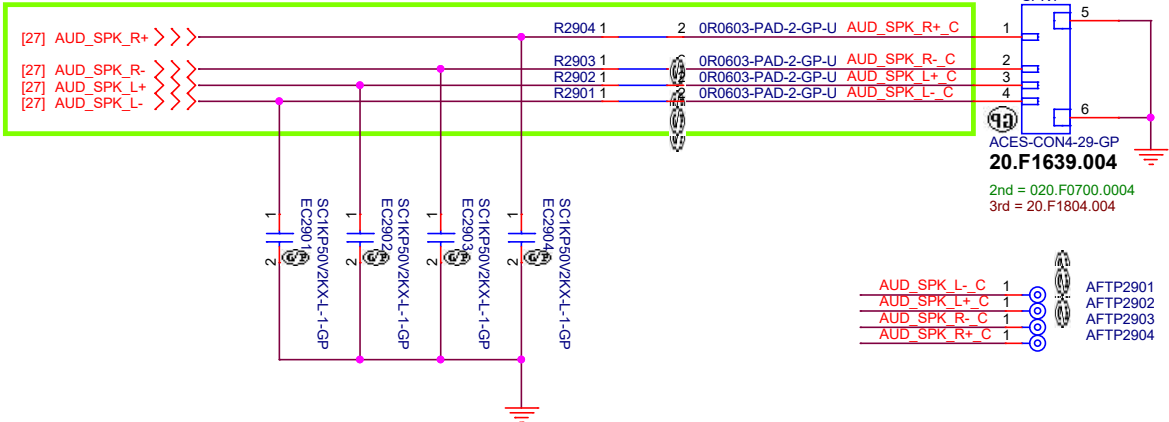
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
(Reserved)			
Size A4	Document Number Vegas SKL/KBL-U		Rev A00
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Main Func = Audio

Layout Note:

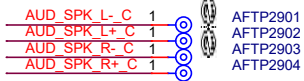
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

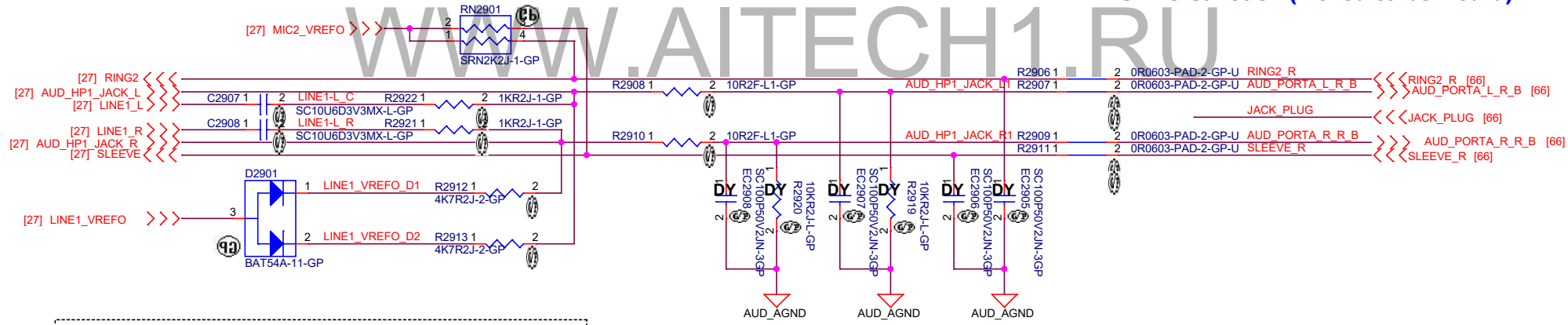


CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

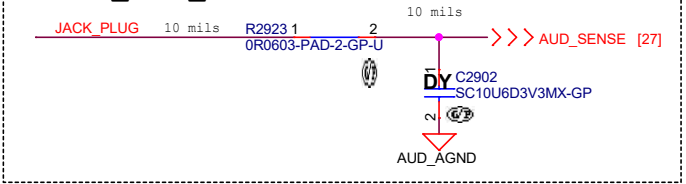
20.F1639.004
2nd = 020.F0700.0004
3rd = 20.F1804.004



Universal Jack (Moved to I/O Board)



Delay circuit
(JACK_PLUG_DET: on IO Board)



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Title

Audio IO

Size	Document Number	Rev
Custom	Turis/Vegas KBL-R	A00
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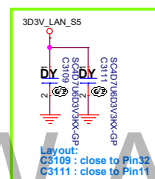
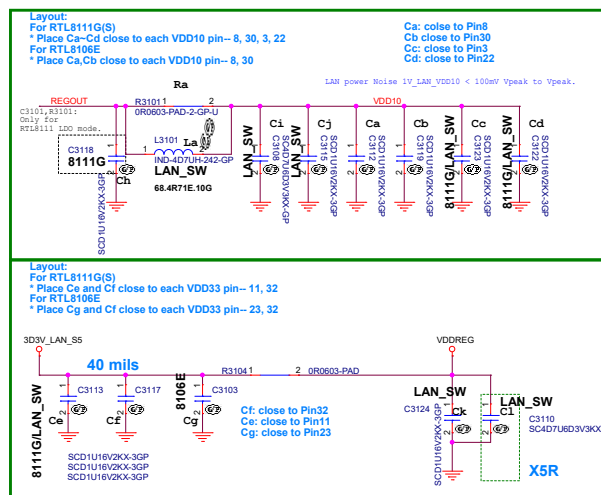
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WWW.AITECH1.RU

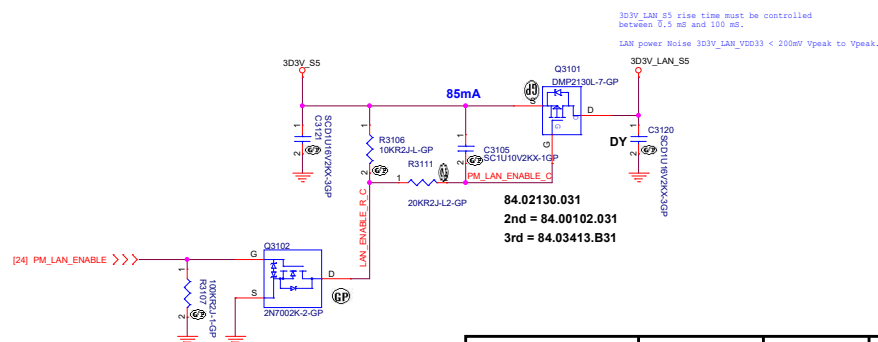
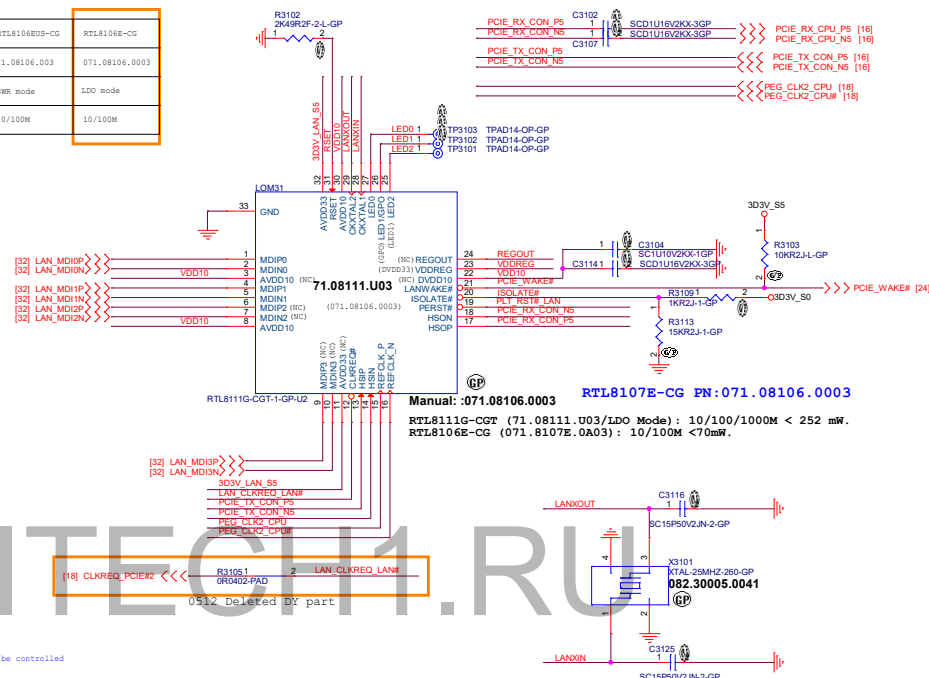
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Title (Reserved)			
Size A4	Document Number Vegas SKL/KBL-U		Rev A00
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Main Func = LAN

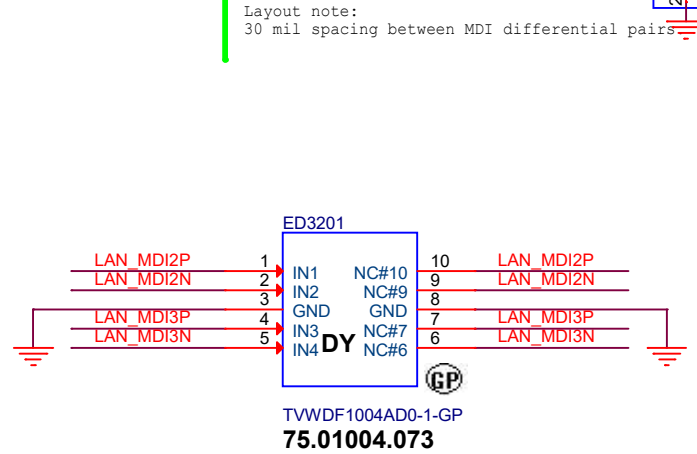
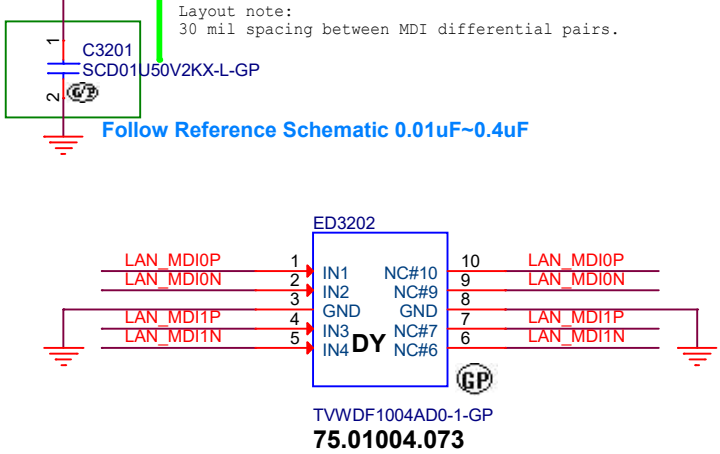
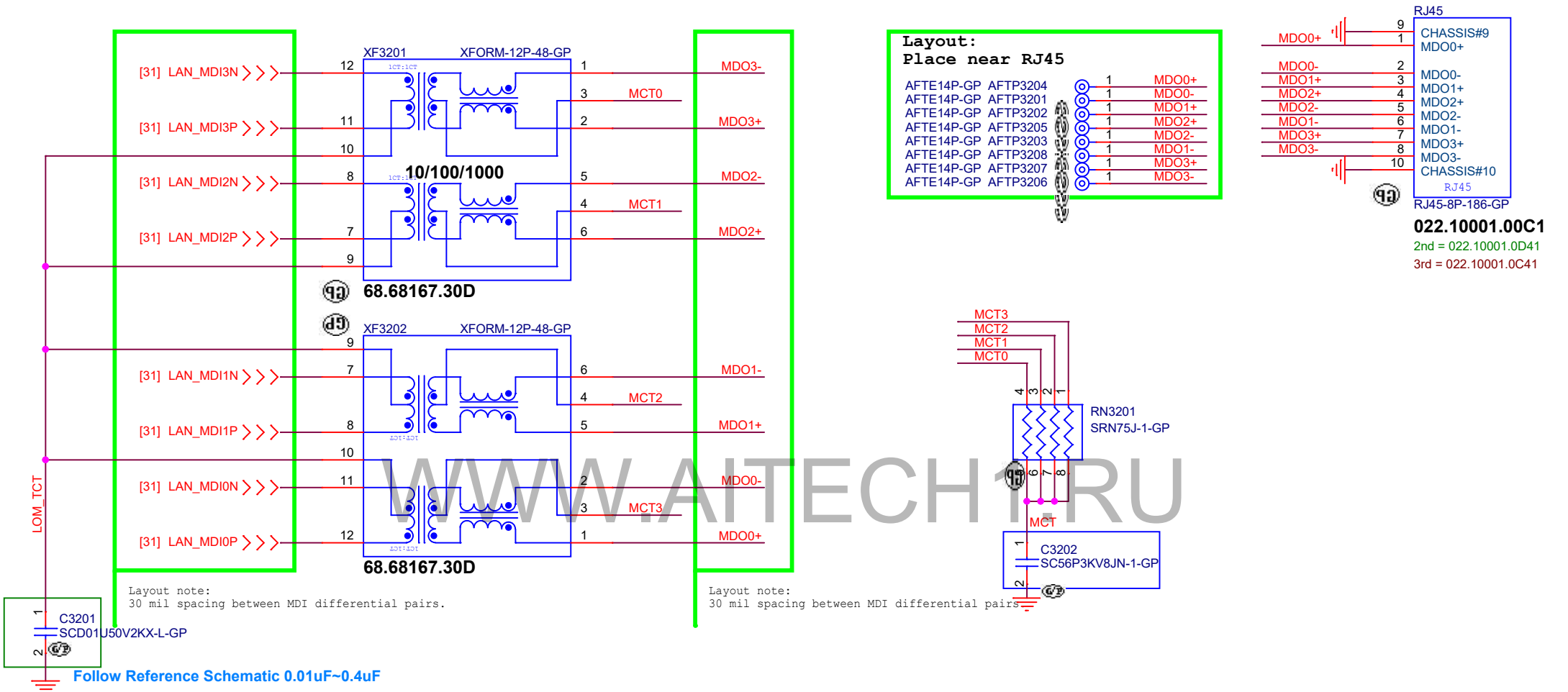


RTL8111GUS-CG	RTL8111G-CGT	RTL8106RUS-CG	RTL8106R-CG
71.08111.W03	71.08111.W03	71.08106.W03	071.08106.W00
SNR mode	LDO mode	SNR mode	LDO mode
10/100/1000M	10/100/1000M	10/100M	10/100M


[illegible]

Main Func = LAN

LAN TransFormer (10/100/1000M & 10/100M co-lay)



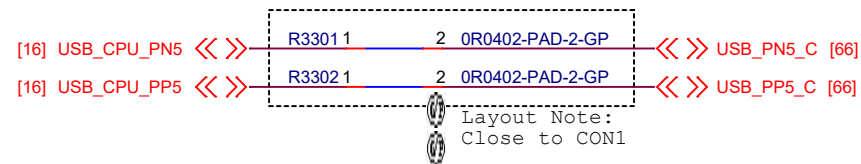
<Core Design>



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Title XFOM&RJ45		
Size A4	Document Number Vegas SKL/KBL-U	Rev A00
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Main Func = Card Reader



WWW.AITECH1.RU

<Core Design>

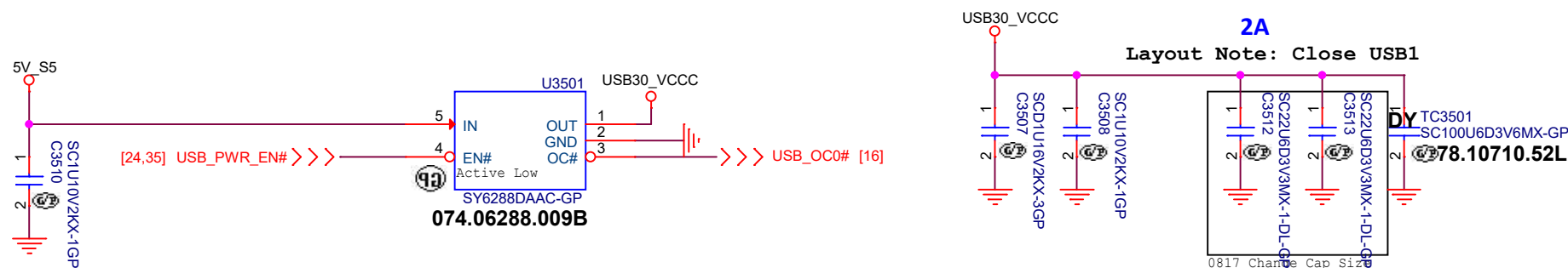
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title Card Reader-RTS5170		
Size A4	Document Number Vegas SKL/KBL-U	Rev A00
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(Blanking)
WWW.AITECH1.RU

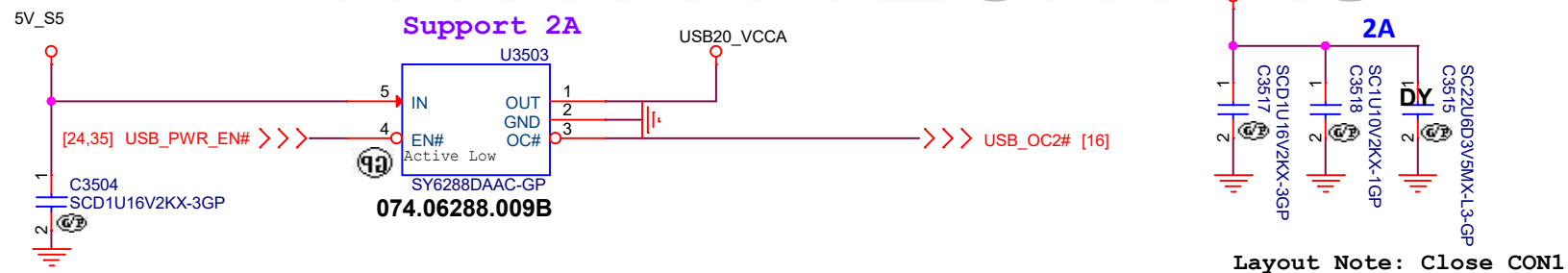
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Title (Reserved)			
Size A4	Document Number Vegas SKL/KBL-U		Rev A00
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Main Func = USB3.0 Port1



Main Func = USB2.0 Port3



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Title

USB switch

Size

Document Number

Turis/Vegas KBL-R

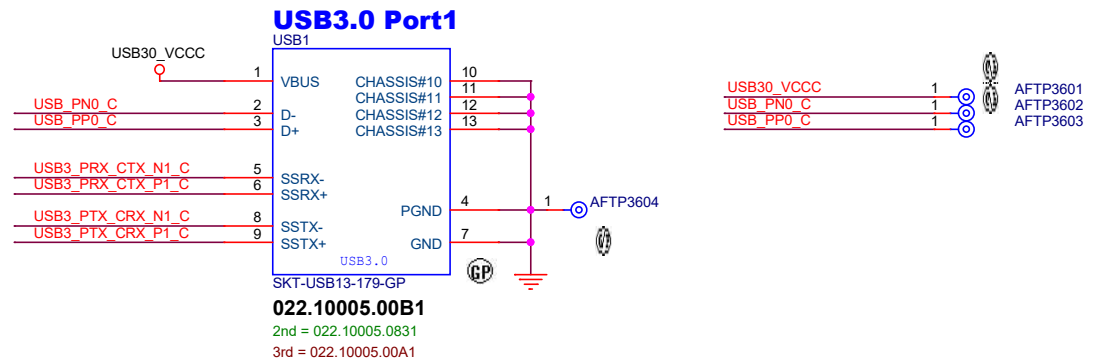
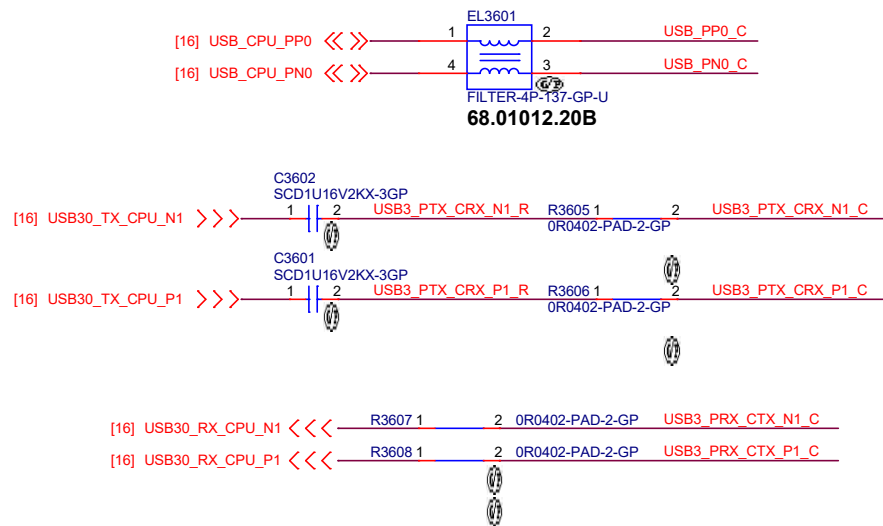
Rev

A00

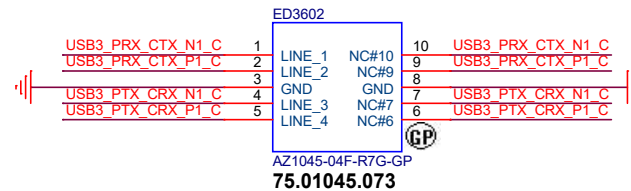
Date: Wednesday, November 08, 2017

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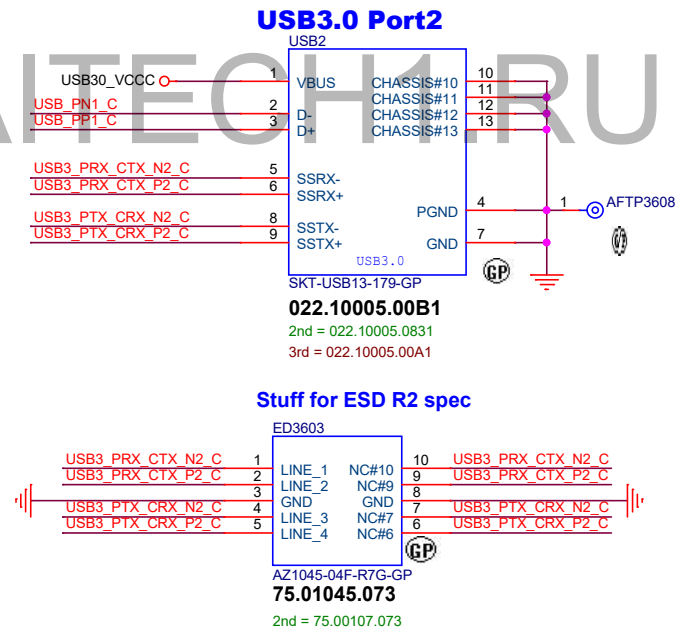
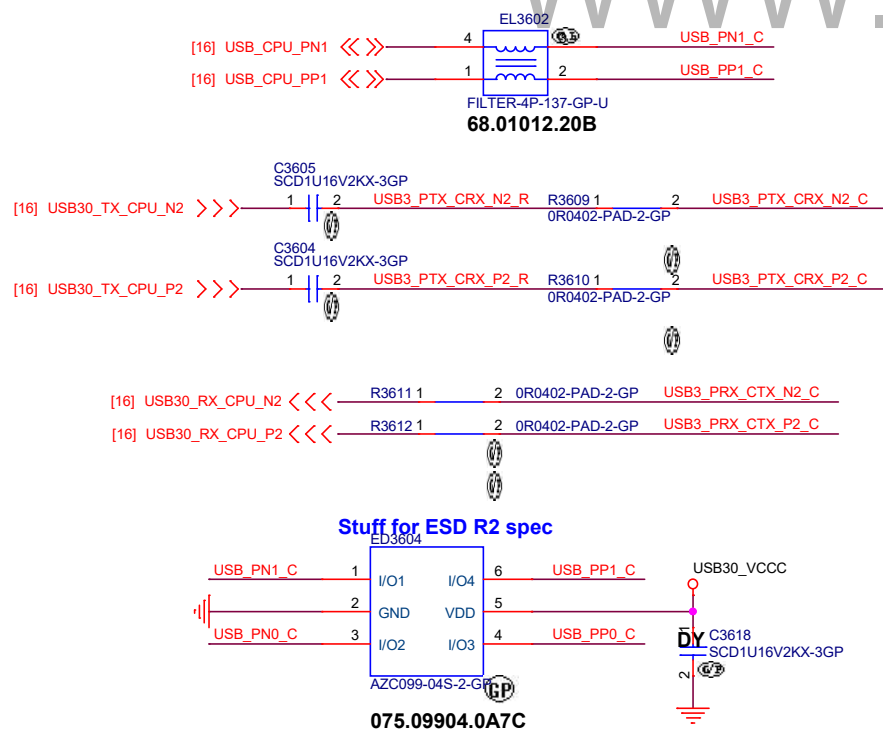
Main Func = USB3.0 Port1



Stuff for ESD R2 spec



Main Func = USB3.0 Port2

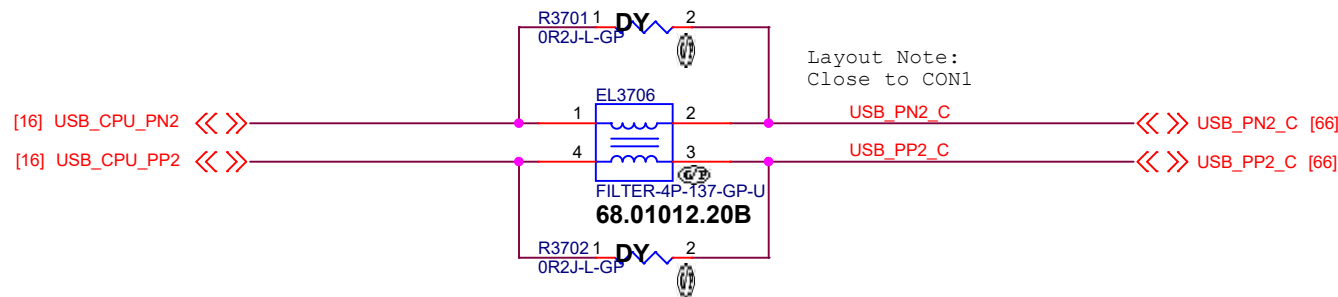


<Core Design>

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB30			
Size	Document Number	Rev	
Custom	Vegas SKL/KBL-U	A00	
Date:	Wednesday, November 08, 2017	Sheet	36 of 105

Main Func = USB2.0 Port3

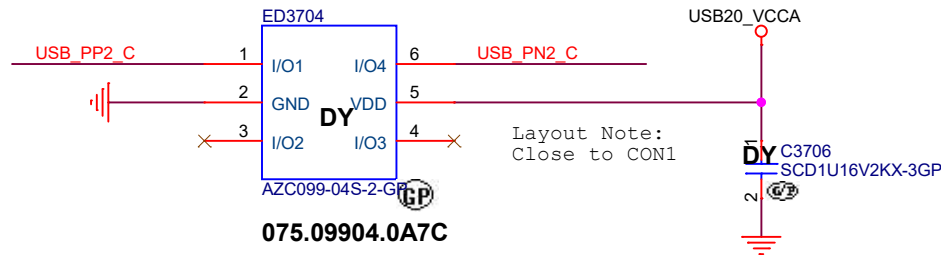
USB port 3 (USB2.0 only) CMC



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USB ESD Diode

Stuff for ESD R2 spec



<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB20			
Size A4	Document Number Turis/Vegas KBL-R		Rev A00
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Vegas SKL/KBL-U		Rev A00
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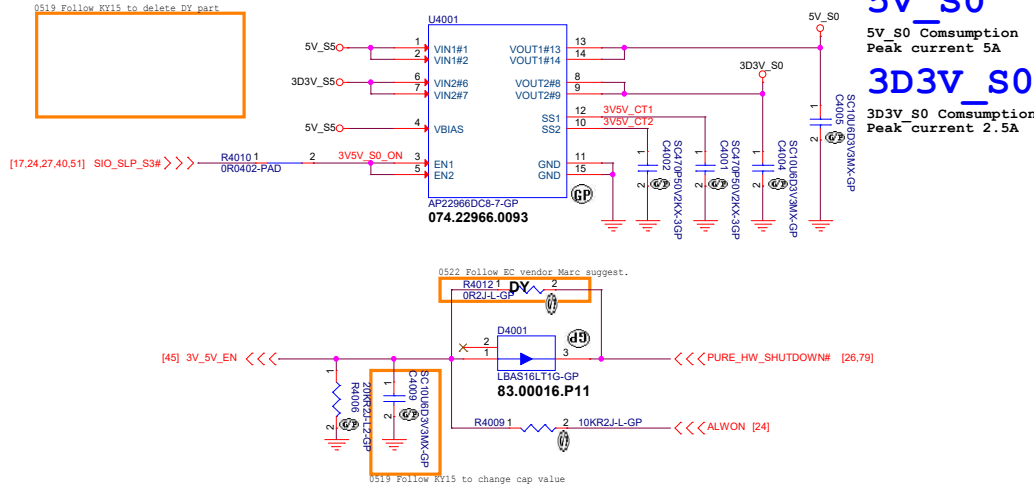
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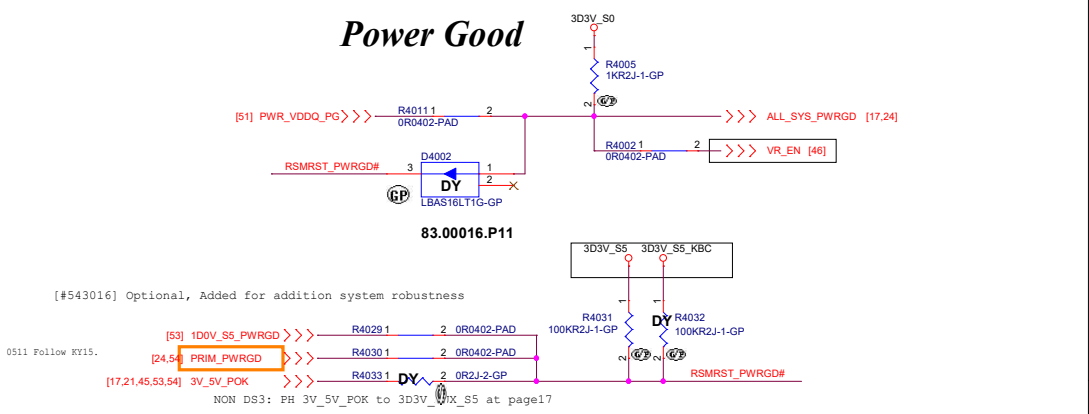
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Title			
(Reserved)			
Size A4	Document Number Vegas SKL/KBL-U		Rev A00
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Main Func = Power Plane & Sequence

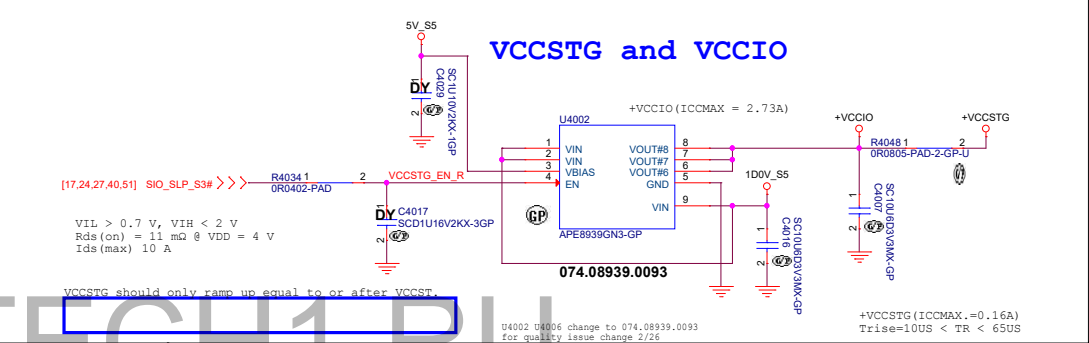
ROSA Run Power



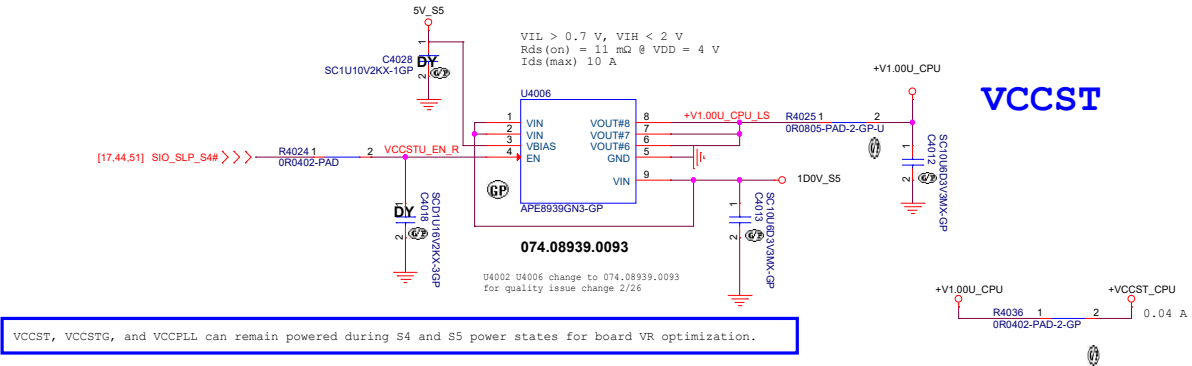
Power Good



VCCSTG and VCCIO



MANAGEMENT RAIL POWER GENERATION



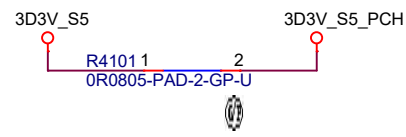
EOPIO and EDRAM

20170428

V1.8S

20170428

Main Func = Power & Sequence



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<Core Design>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <i>Connected_Standby(1/2)+DS3</i>					
Size A4		Document Number <i>Vegas SKL/KBL-U</i>			Rev <i>A00</i>
Date: Wednesday, November 08, 2017		Sheet 41		of 105	

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WWW.AITECH1.RU

<Core Design>



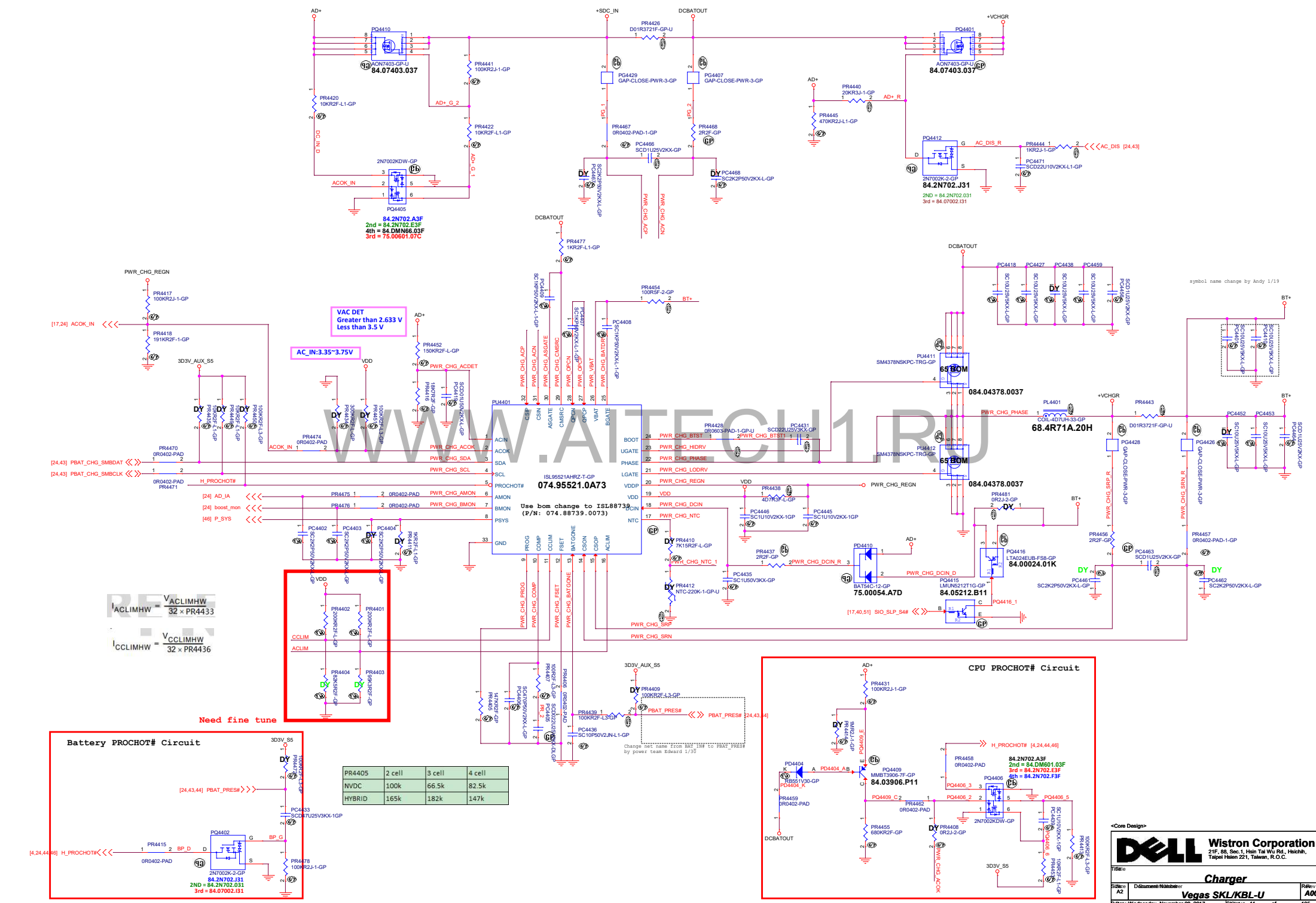
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **Connected_Standby(2/2)**

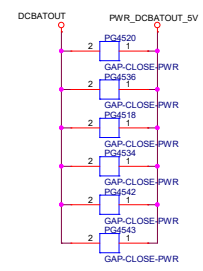
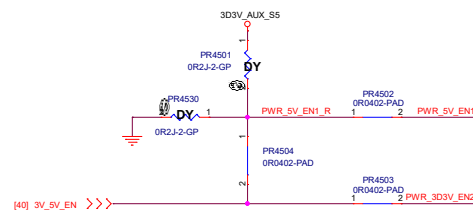
Size A4	Document Number Vegas SKL/KBL-U	Rev A00
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Main Func = Charger



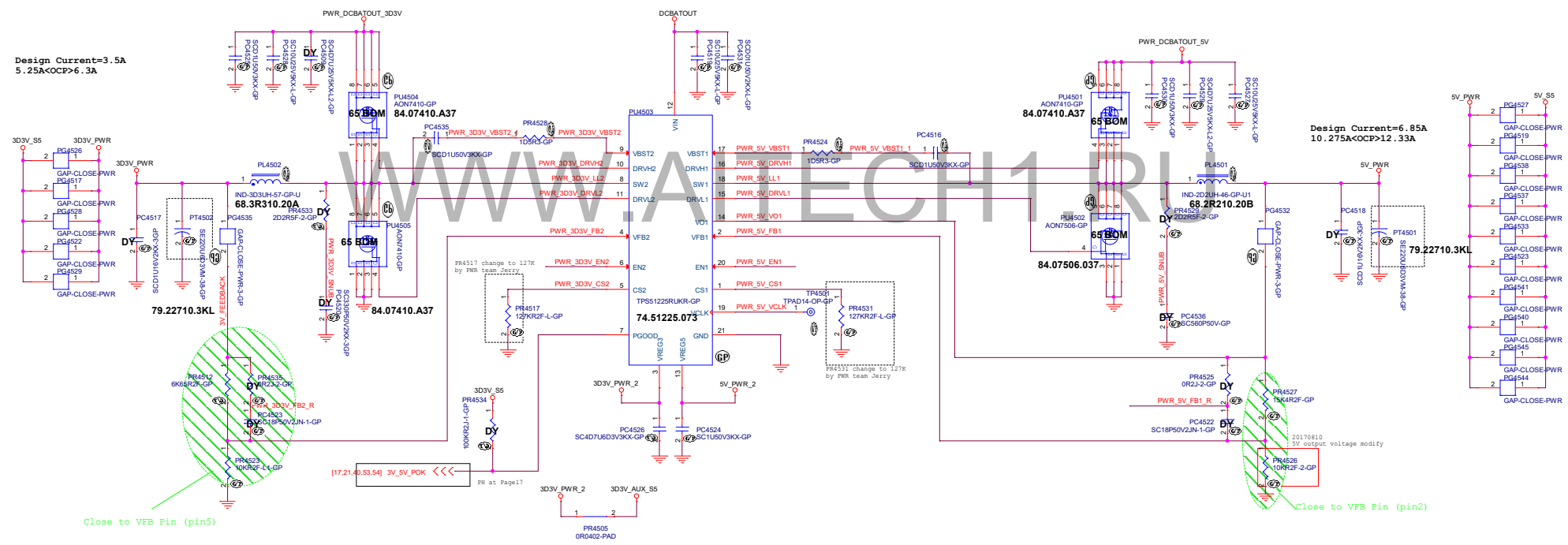
Main Func = 3D3V_5V



Change PU4503 from 074.06575.0A to 74.51225.073 by power change 2/26

Design Current=3.5A
5.25A<OCP>6.3A

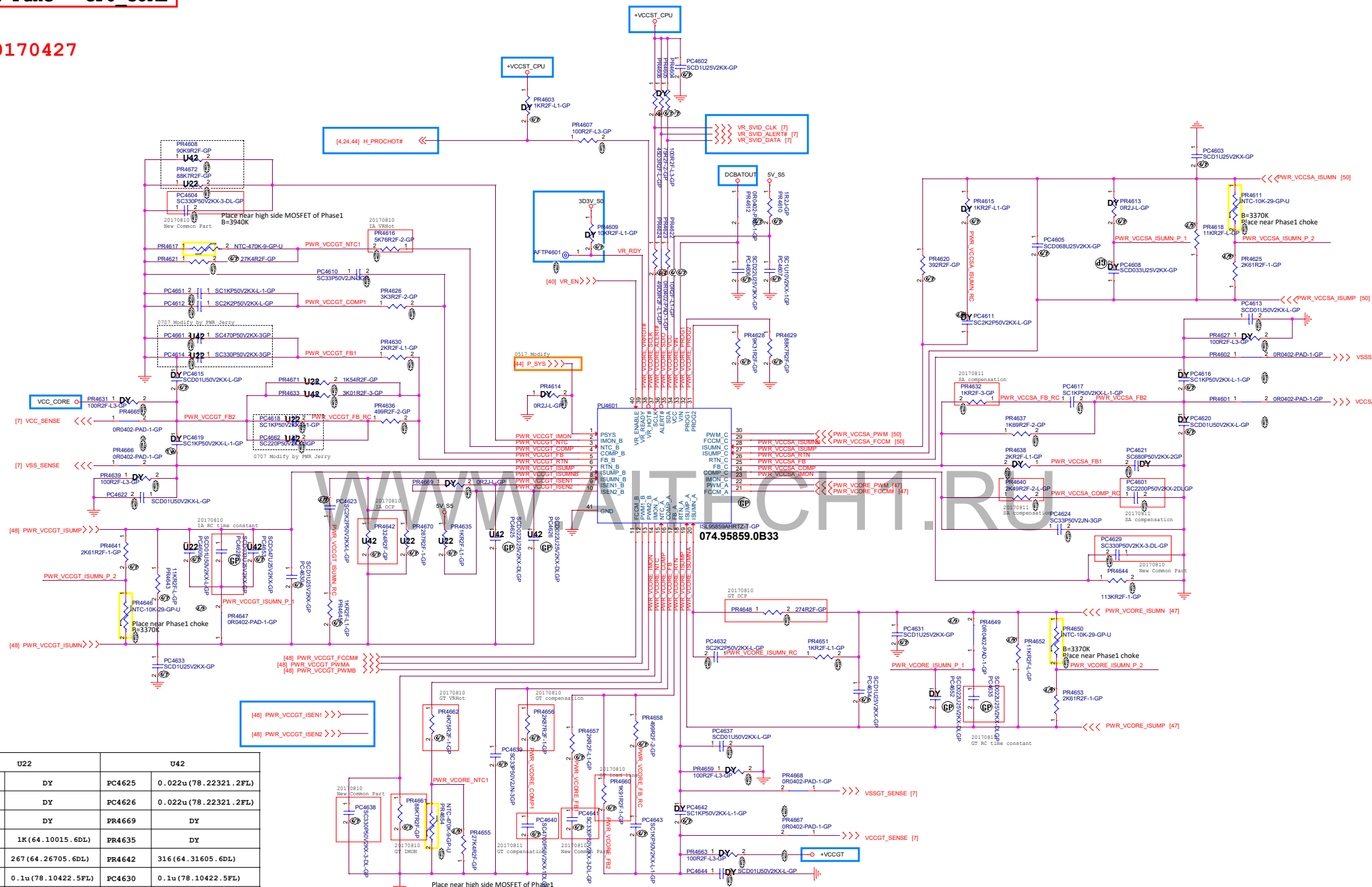
Design Current=6.85A
10.275A<OCP>12.33A



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P capCHIP CAP EL 220U 6.3V M6.3*4.4 /ChemI-con/ 18mohm / 79.22710.3KL
H/S: SIS412 / 24mohm/30mohm@4.5Vgs / 84.00412.037
L/S: SIS412 / 24mohm/30mohm@4.5Vgs / 84.00412.037

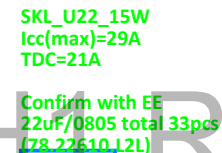
I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOK 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P capCHIP CAP EL 220U 6.3V M6.3*4.4 /ChemI-con/ 18mohm / 79.22710.3KL
H/S: SIS412 / 24mohm/30mohm@4.5Vgs / 84.00412.037
L/S: SIS780 / 14.5mohm/17.5mohm@4.5Vgs / 84.00780.037

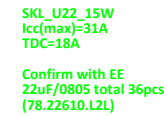
20170427



U22		U42	
PC4625	DY	PC4625	0.022u (78.22321.2FL)
PC4626	DY	PC4626	0.022u (78.22321.2FL)
PR4669	DY	PR4669	DY
PR4635	1K (64.10015.6DL)	PR4635	DY
PR4670	267 (64.26705.6DL)	PR4642	316 (64.31605.6DL)
PC4630	0.1u (78.10422.5FL)	PC4630	0.1u (78.10422.5FL)
PC4609	0.01u (78.10324.10L)	PC4628	0.022u (78.22322.2FL)
PC4653	DY	PC4653	47n (78.47322.2FL)
PR4671	1.54K (64.15415.6DL)	PR4633	3.01K (64.30115.6DL)
PR4672	88.7K (64.88725.6DL)	PR4608	90.9K (64.90925.6DL)
PC4614	330p (78.33124.2FL)	PC4661	470p (78.47124.2FL)
PC4618	1000p (78.10224.2FL)	PC4662	220p (78.22124.2FL)

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CGTB

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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title NCP81210MN_CPU_VCCGTUS		
Size A4	Document Number Vegas SKL/KBL-U	Rev A00
Date: Wednesday, November 08, 2017		Sheet 49 of 105

5

4



1

1

1



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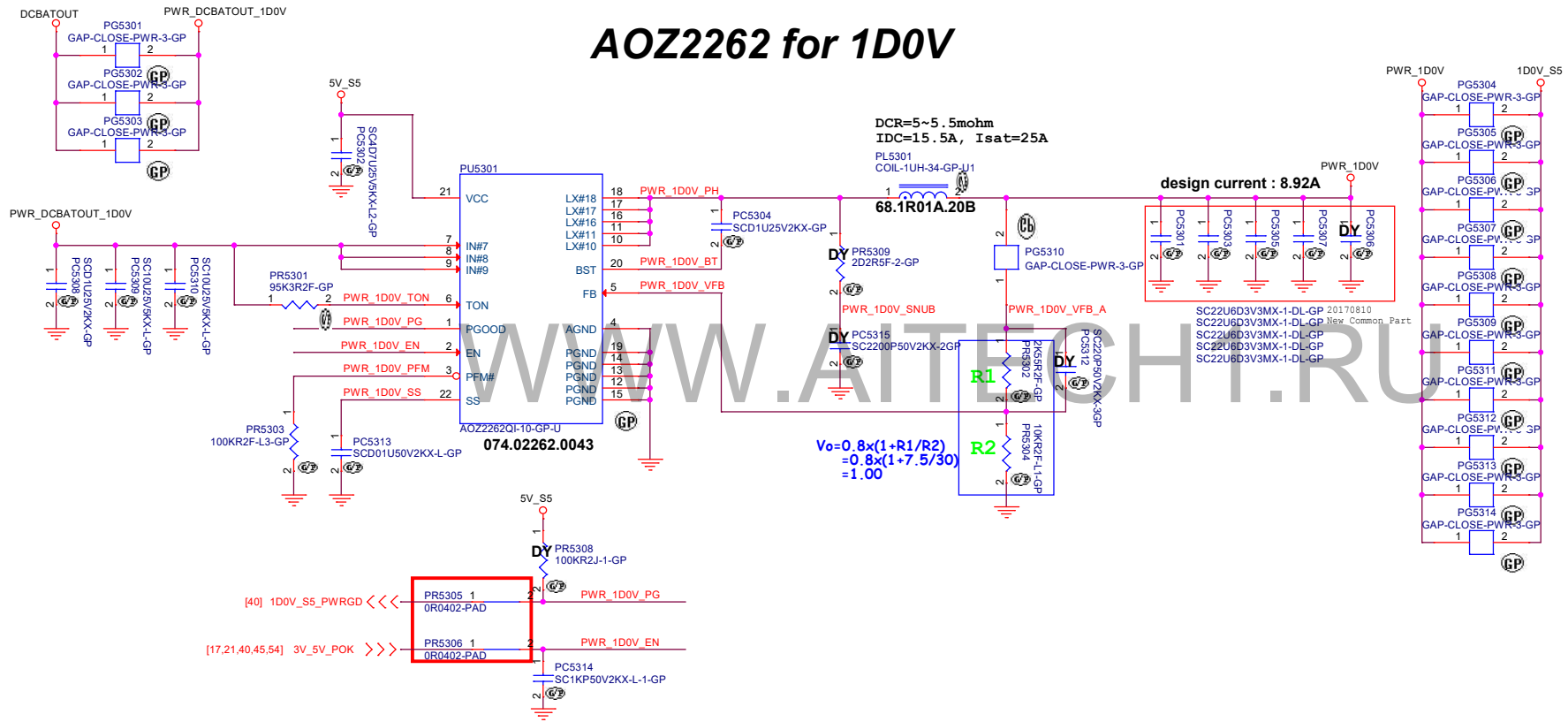
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
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SSID = PWR.Plane.Regulator_1p0v

AOZ2262 for 1D0V

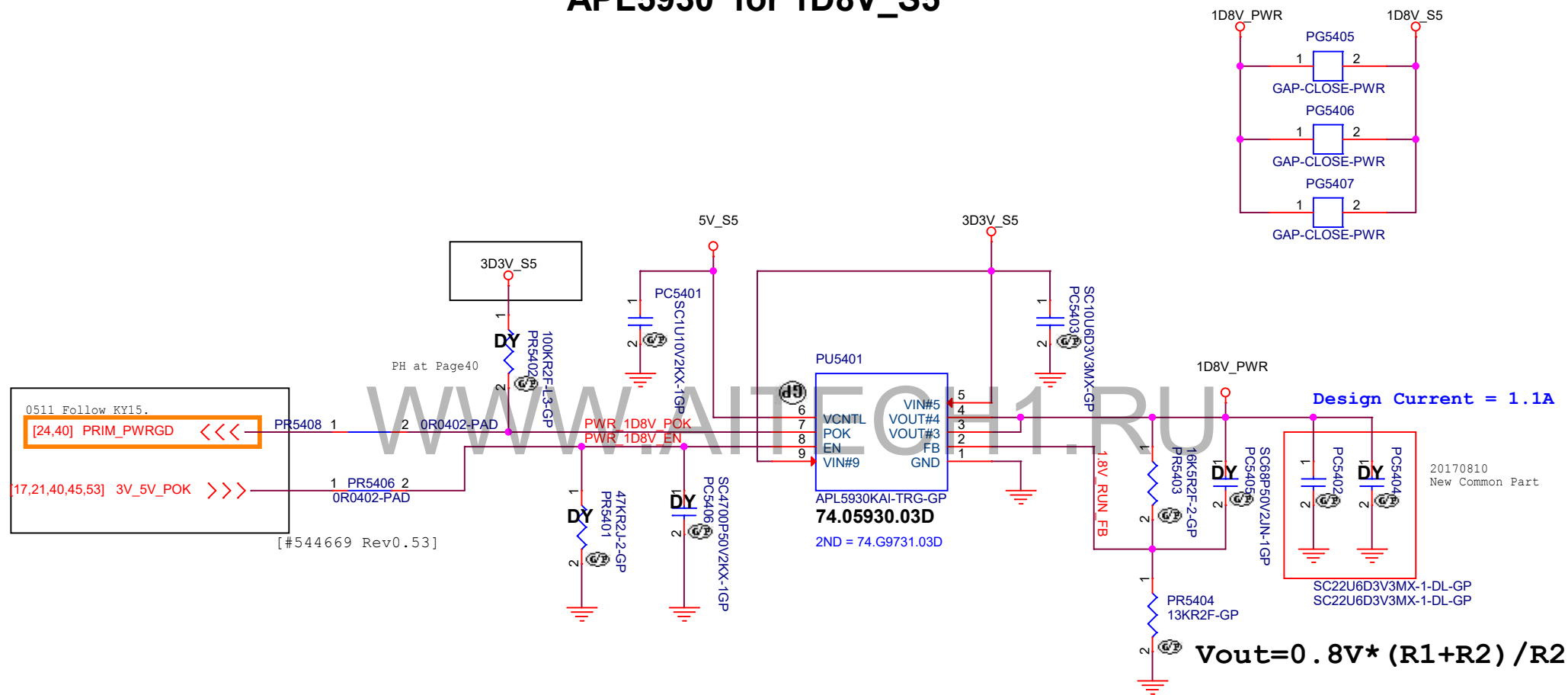


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DELL Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title AOZ2262QI_1D0V		
Size Custom	Document Number Vegas SKL/KBL-U	Rev A00
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Main Func = 1D8V

APL5930 for 1D8V_S5



<Core Design>



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Title

LDO-V1D5V&V1D8V

Size
A4

Document Number

Vegas SKL/KBL-U

Rev
A00

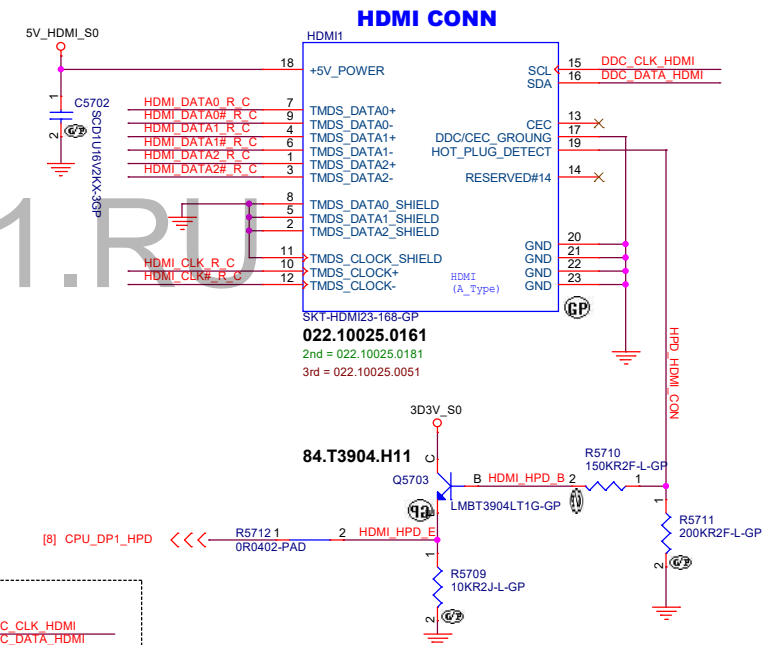
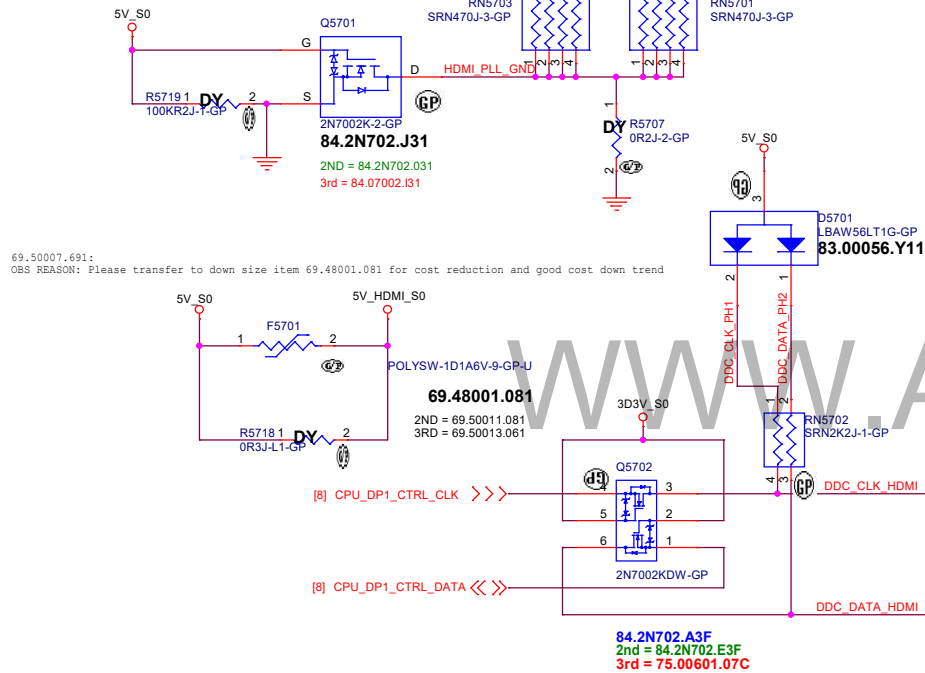
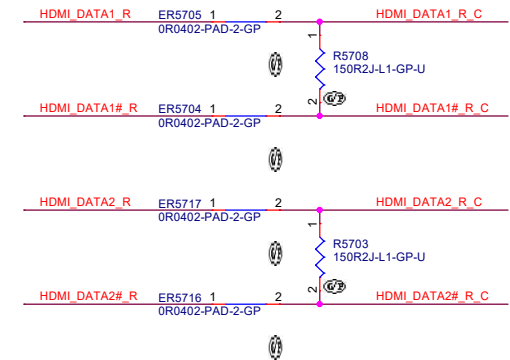
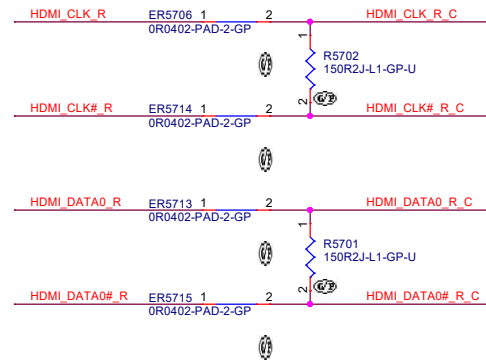
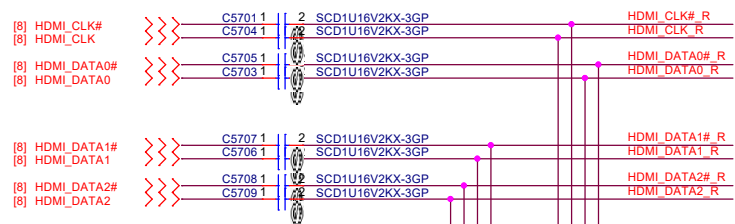
Date: Wednesday, November 08, 2017

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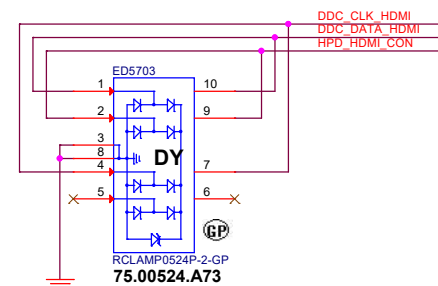
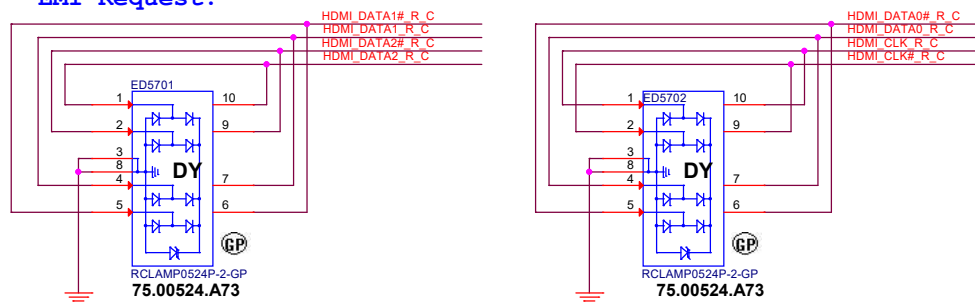
of

105

Main Func = HDMI



EMI Request:



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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

(Blanking)

Size

A4A4

Document Number

Vegas 941 841/MBL-U

Rev

A00

Date: Wednesday, November 08, 2017

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<Core Design>



Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Display (RSVD)

Size
A4

Document Number

Vegas SKL/KBL-U

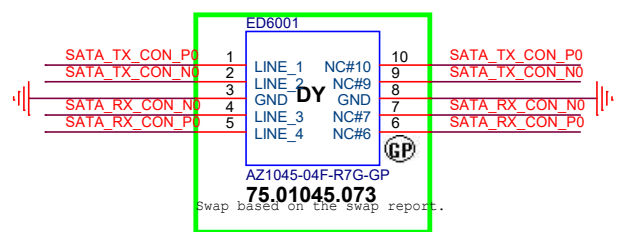
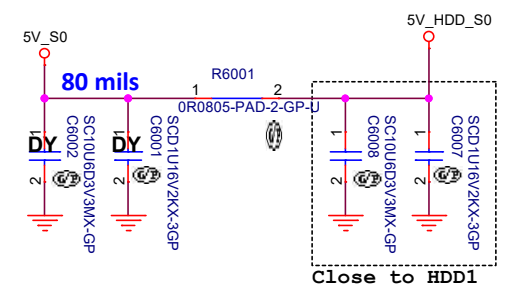
Rev
A00

Date: Wednesday, November 08, 2017

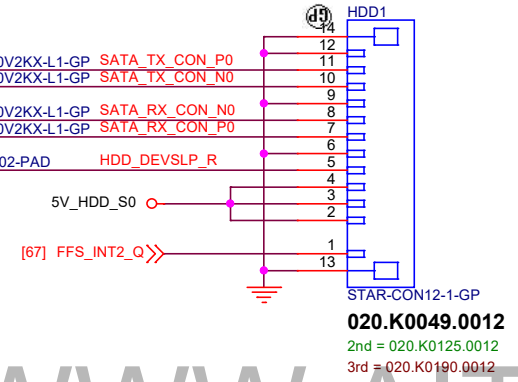
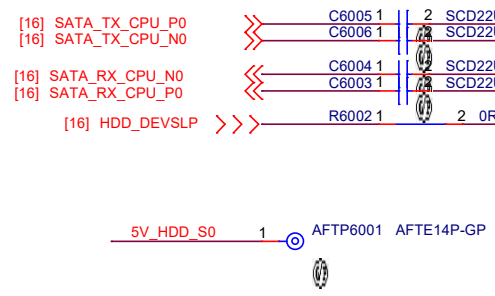
Sheet 59 of 105

Main Func = HDD

SATA HDD Connector



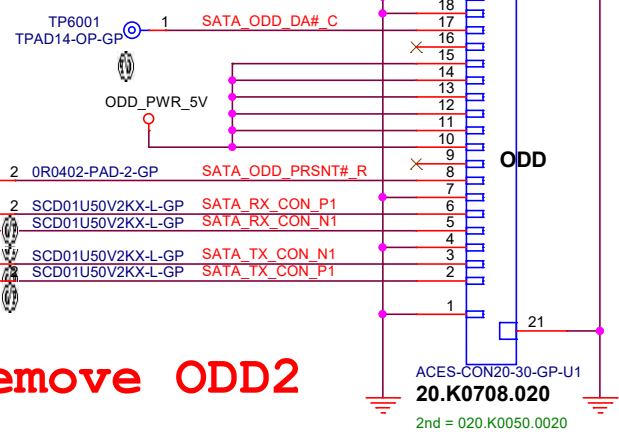
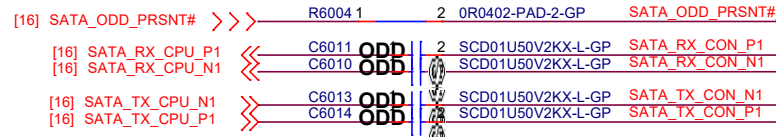
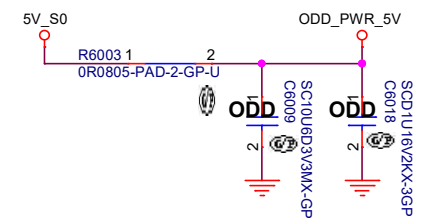
Layout Note:
Place near HDD1



CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	

Main Func = ODD

ODD Connector



20170502 remove ODD2

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title
INT IO (HDD/ODD)

Size
Custom

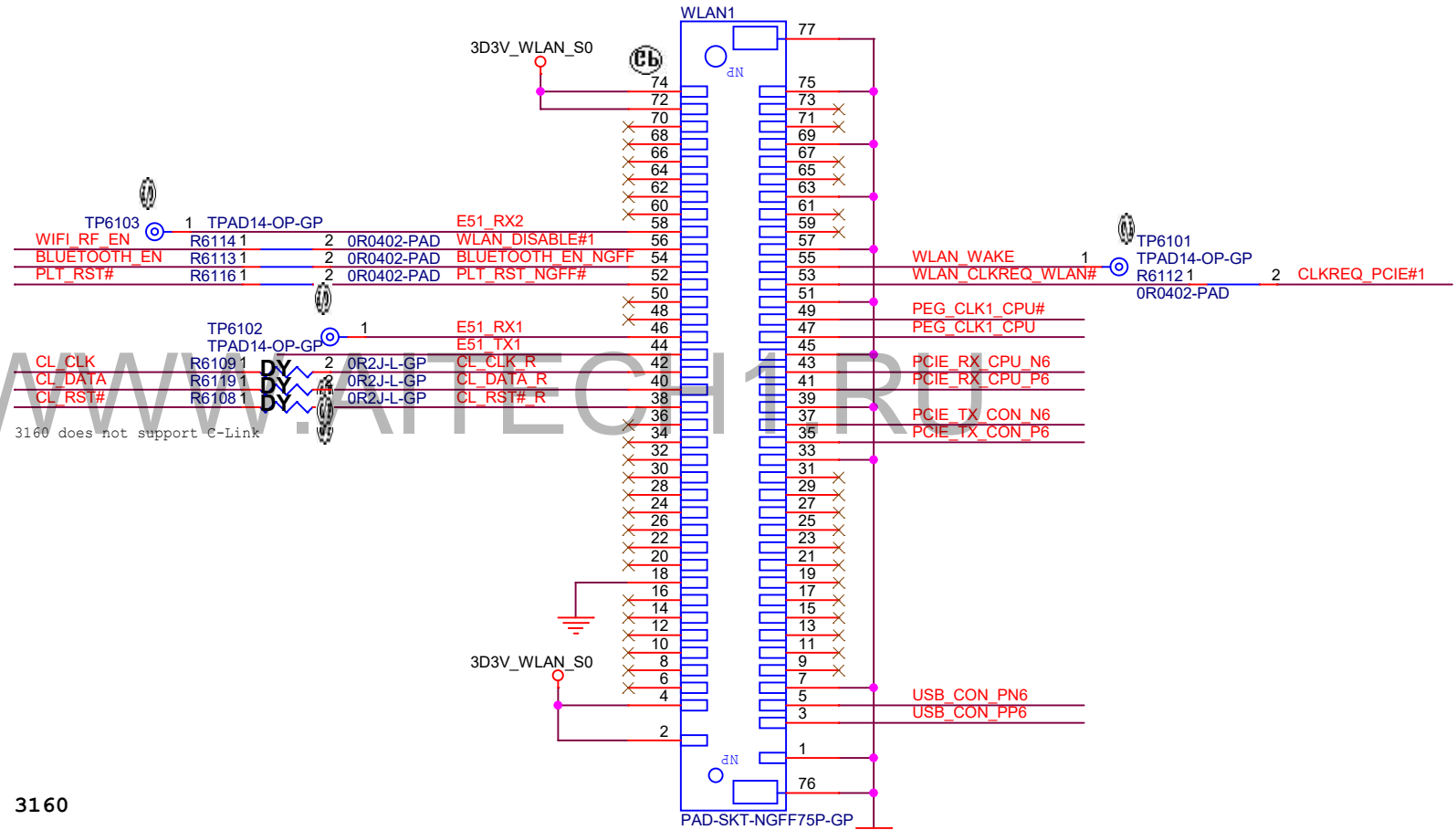
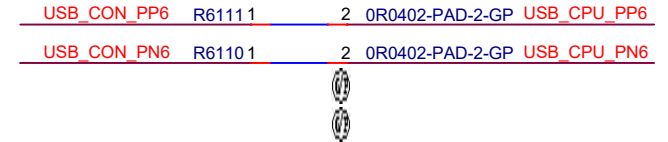
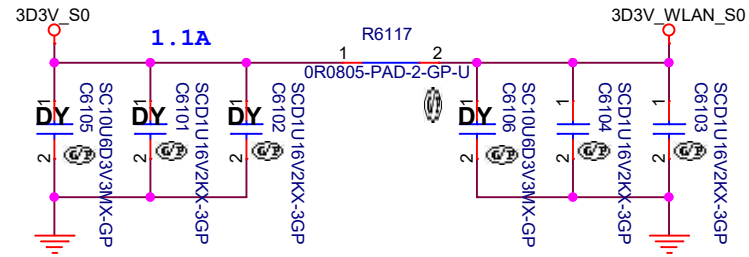
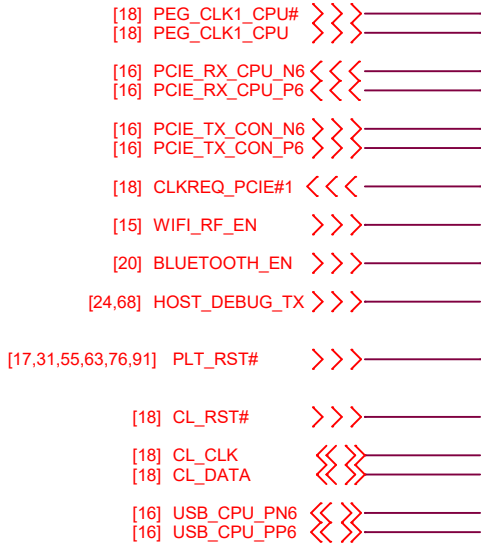
Document Number
Vegas SKL/KBL-U

Rev
A00

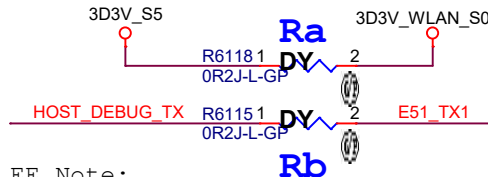
Date: Wednesday, November 08, 2017

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Main Func = WLAN

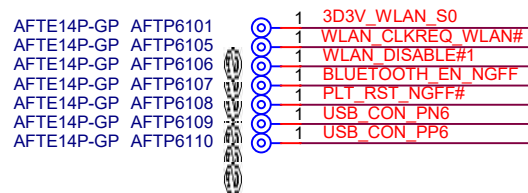


Reserved for NGFF Debug Card



EE Note:
For NFGG Debug Card:
Stuff Ra, Rb; DY Rc.
Note:pin 76 and pin 77 need contact to GND

Support: Intel Dual Band Wireless-AC 3160



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Title

NGFF WLAN CONN

Size
A4

Document Number

Vegas SKL/KBL-U

ev

A00

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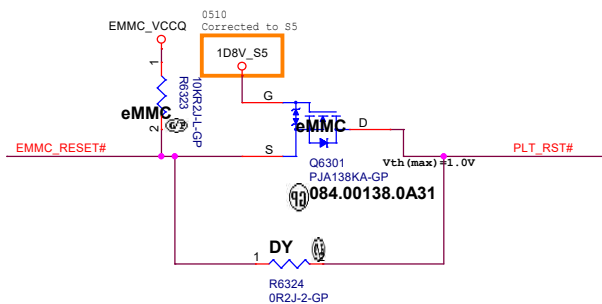
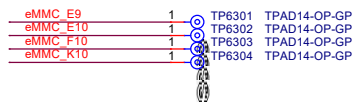
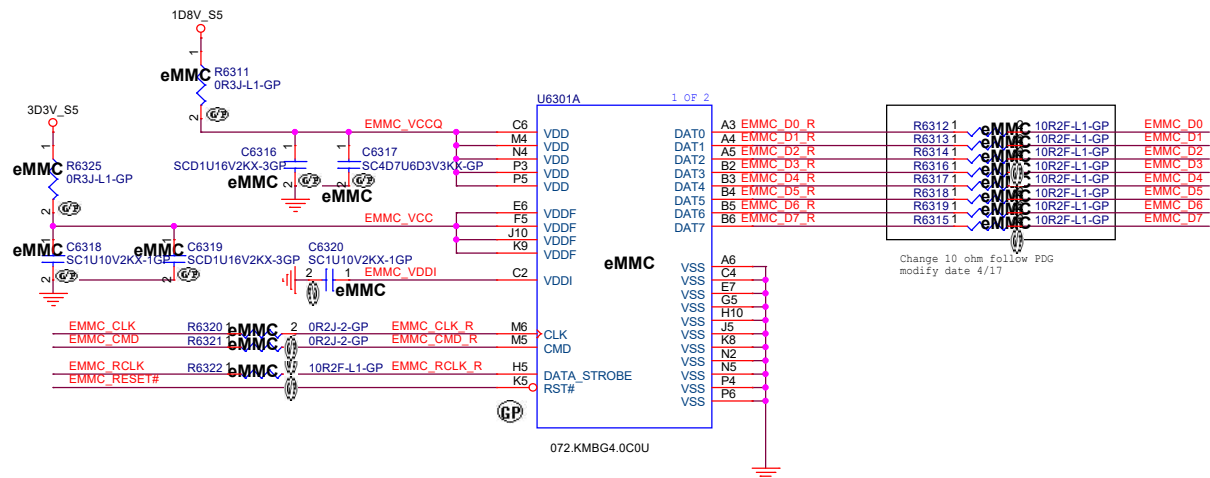
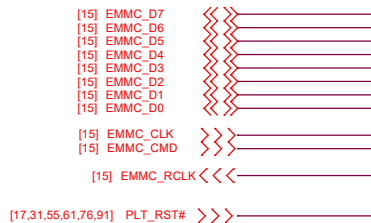
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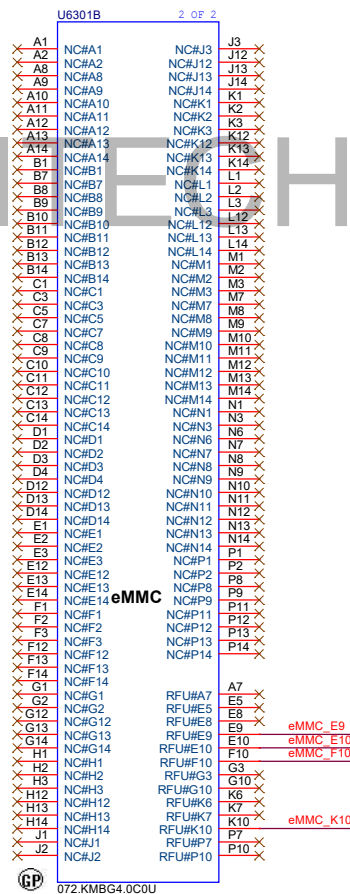
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Title			
Reserved			
Size A4	Document Number Vegas SKL/KBL-U		Rev A00
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Main Func = eMMC

EMMC



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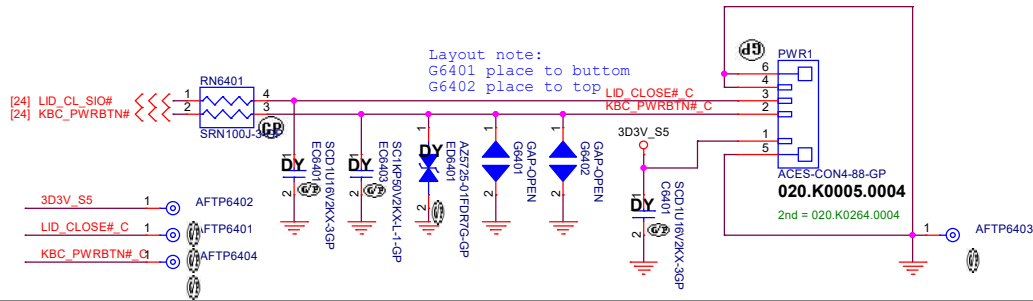


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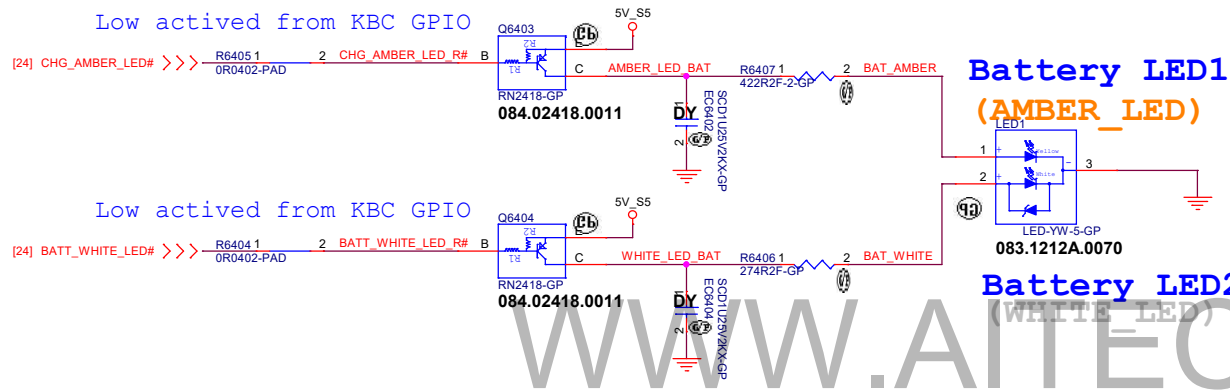
DELL Wistron Corporation
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Size	Document Number	Rev
A3	Vegas SKL/KBL-R	A00
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Power button

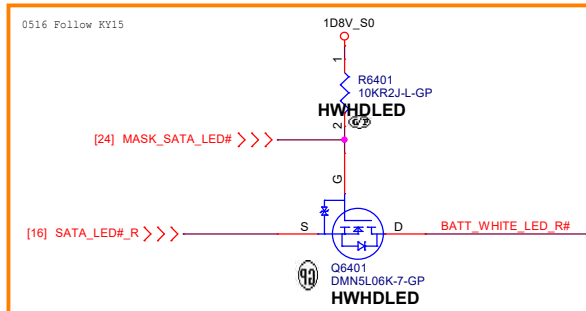


Main Func = Battery LED



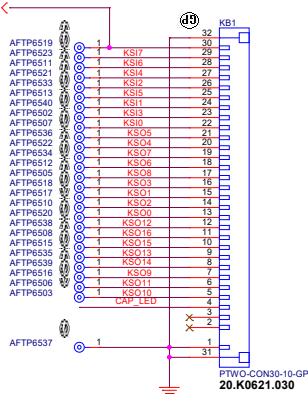
Main Func = HDD LED

SATA HDD LED
LOW actived from **PCH GPIO**



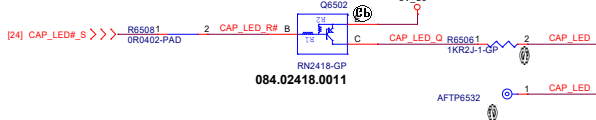
Main Func = KB

Internal Keyboard Connector



CAP LED Control

LOW acted from KBC GPIO

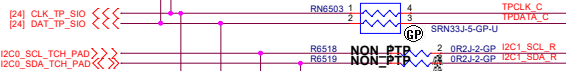


0502 Deleted KB2
0524 Deleted KBBL1 block

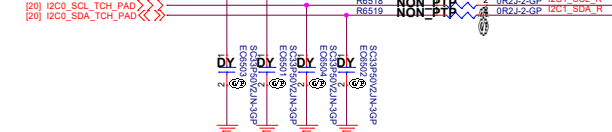
Main Func = TPAD

Support PTP

PS2

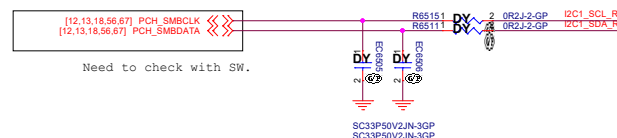


I2C

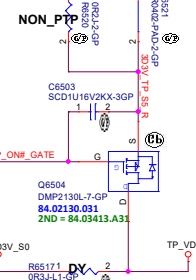


Vages install Non PTP

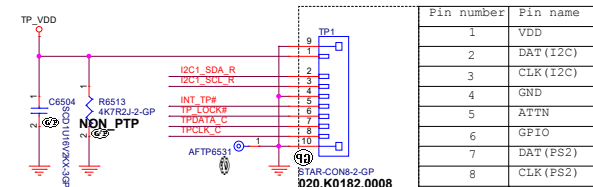
SMBUS



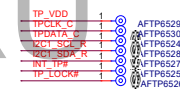
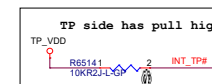
Need to check with SW.



Precision Touch Pad Connector

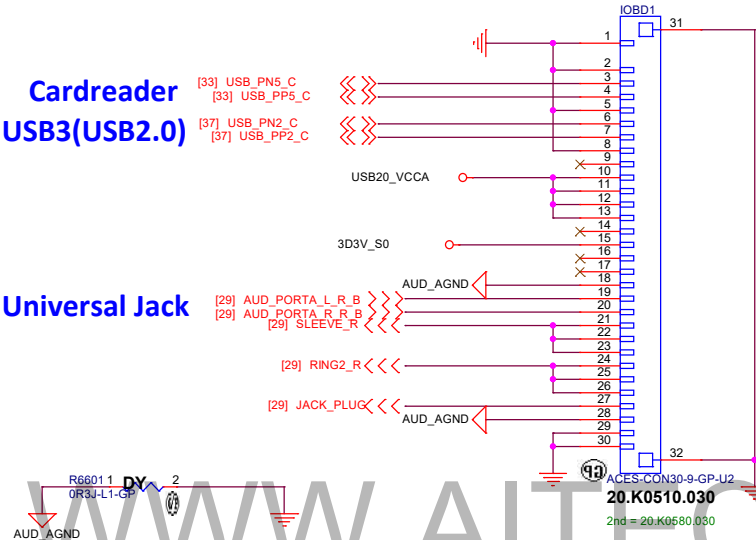


Need to check if it is Active High or Active Low and check if there is PH on TPAD side.

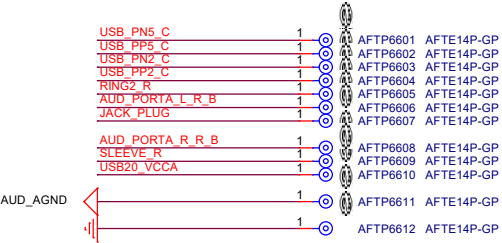


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I/O Board Connector



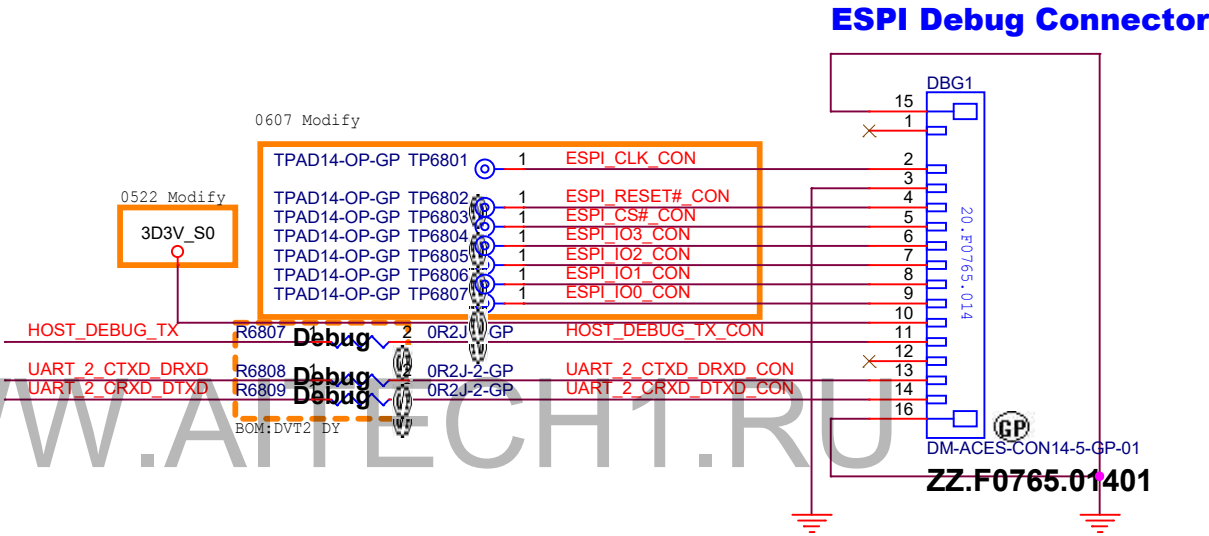
Pitch: 1mm
Power: 6 pins
GND: 7 pins
AGND: 2 Pins



Main Func = Debug

UART

[24,61] HOST_DEBUG_TX >>>
[20] UART_2_CTXD_DRXD >>>
[20] UART_2_CRXD_DTXD <<<



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Dubug connector

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USB3.0 PORT

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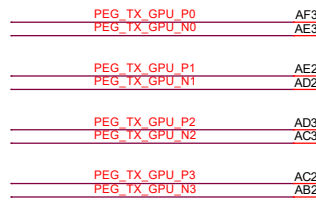
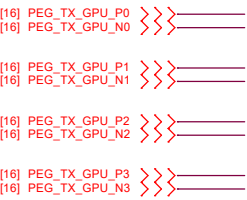
Vegas SKL/KBL-U

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20170502



GFX & GPP, 85Ω
GFX & GPP CLK, 85Ω

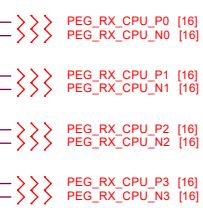
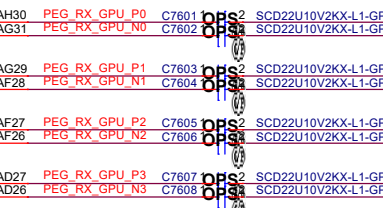
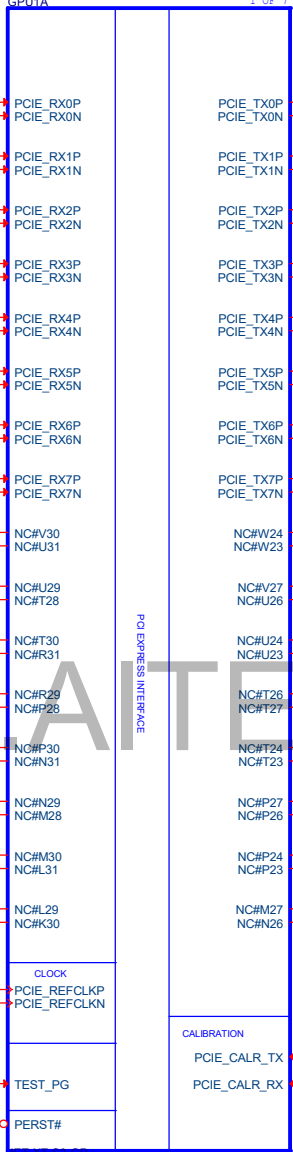
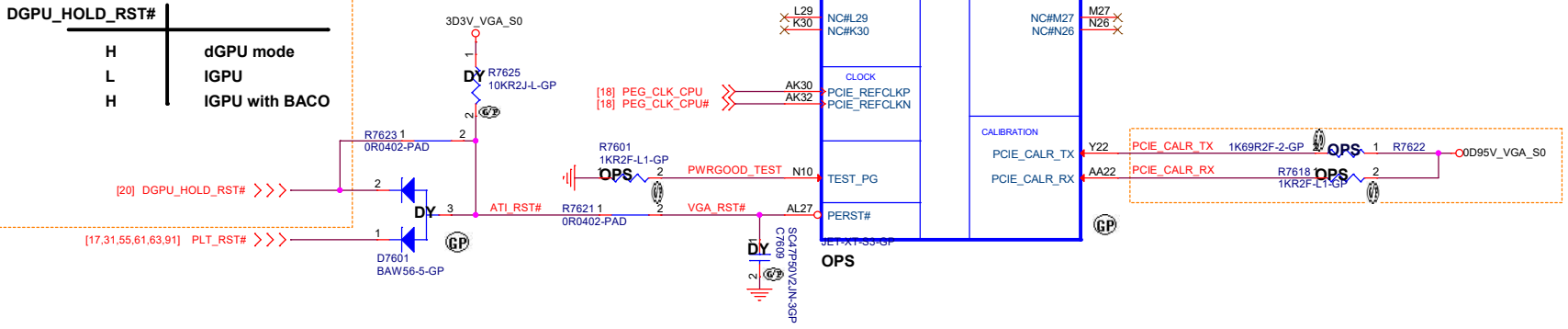


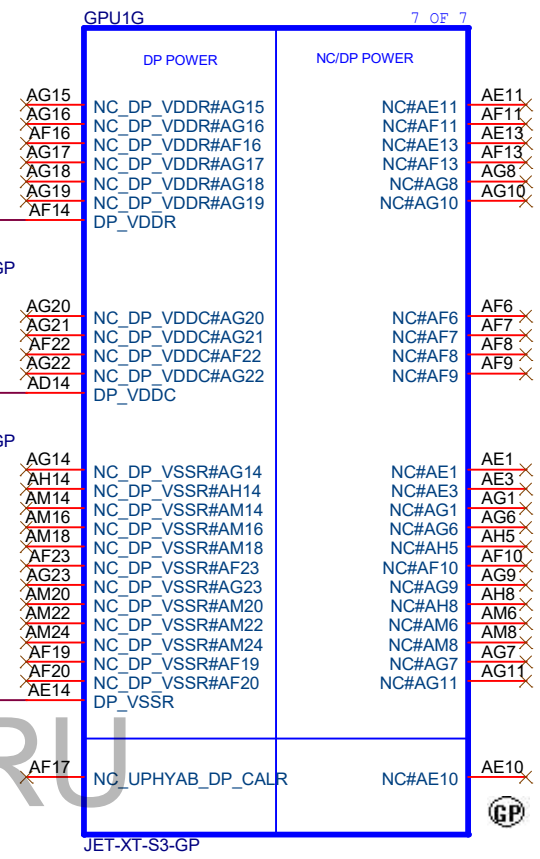
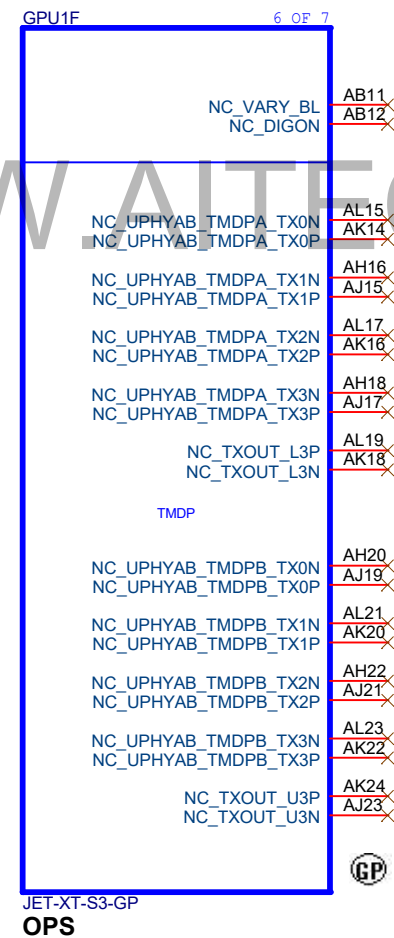
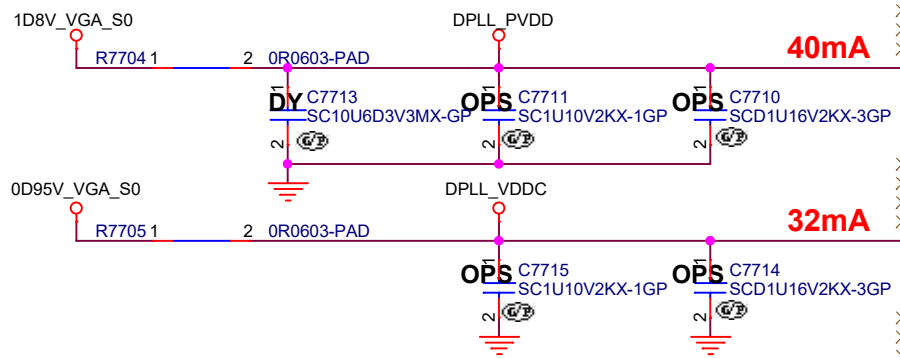
Table 3-5 PCI Express® Bus Interface

Pin Name	I/O	Description
PERSTb	I	Fundamental reset. 3.3-V tolerant pad. This signal must be asserted during any fundamental reset event, such as power up, warm boot, reset button pressed, CTL-ALT-DEL, Windows restart, or wake from D3.
PCIE_REFCLKP/N	I	PCI Express PLL differential reference clock (+/-). 100-MHz (± 300 ppm) input frequency; 0-V to 0.7-V single-ended swing.
PCIE_TX[7:0]P/N	O	PCI Express transmitter output data channel TX[7:0] (+/-). Differential serial data transmitted up to a 8.0-GT/s bit rate.
PCIE_RX[7:0]P/N	I	PCI Express receiver input data channel RX[7:0] (+/-). Differential serial data received up to a 8.0-GT/s bit rate.
PCIE_CALR_RX	I	Connect to PCIE_VDDC through a 1-kΩ (1% tolerance) resistor.
PCIE_CALR_TX	I	Connect to PCIE_VDDC through a 1.69-kΩ (1% tolerance) resistor.
CLKREQB	O	Reserved, do not connect on the PCB.

DGPU_HOLD_RST#	
H	dGPU mode
L	IGPU
H	IGPU with BACO

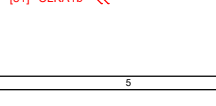
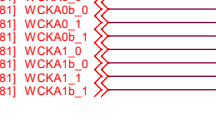
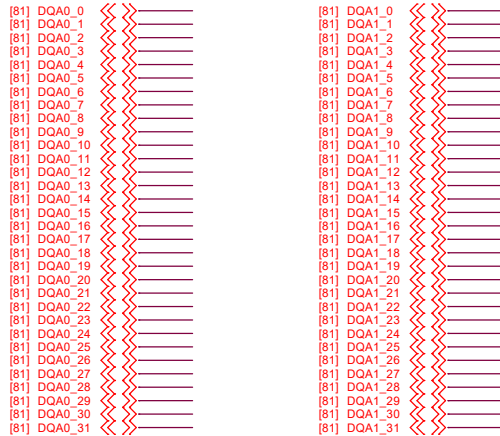


Main Func = dGPU



BALL: AB11, AB12
R16 : NC
MESO : VDDC

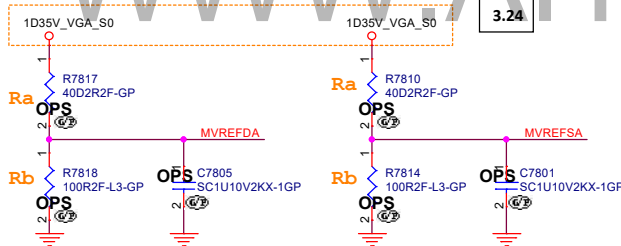
Main Func = dGPU



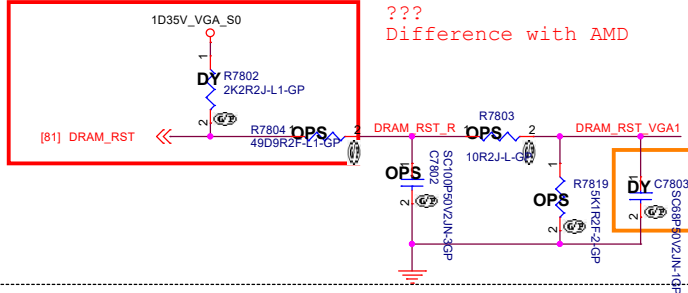
Please MVREF drivers and Caps close to ASIC

DDR3/GDDR3 Memory Stuff Option(R16)

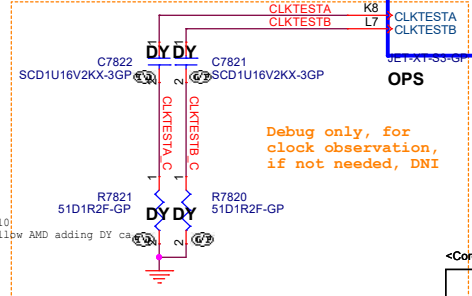
	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1D35V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R



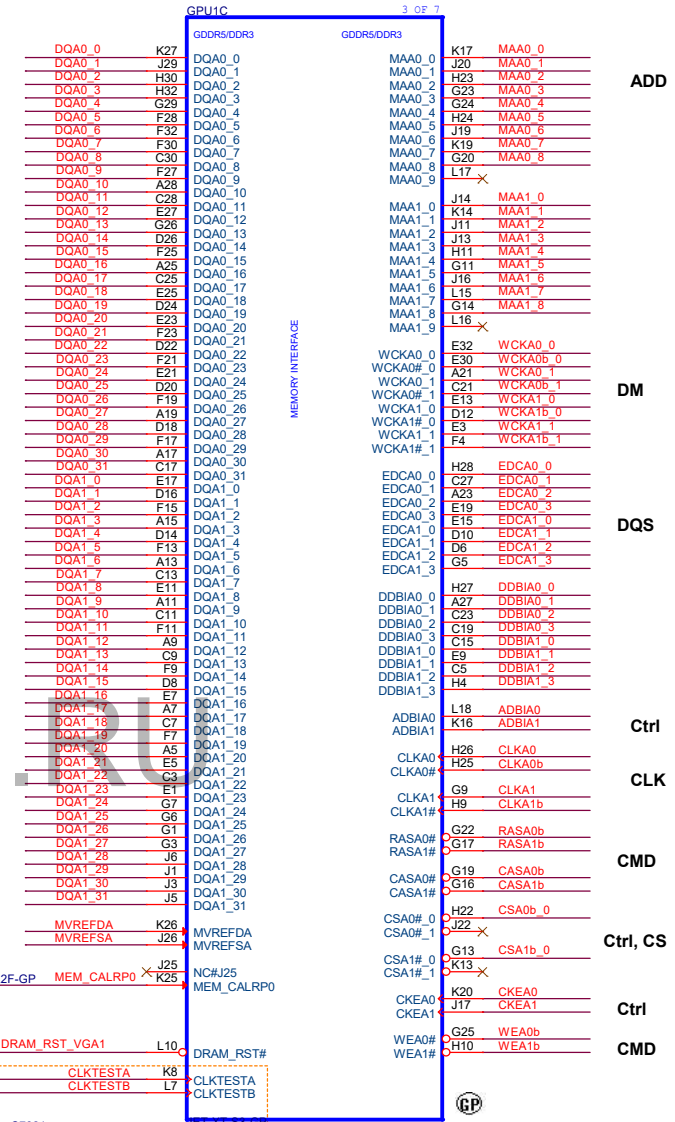
Place all these componets very close to GPU (within 25mm) and keep all componets close to each other
This basic topology should be used for DRAM_RST for DDR3/GDDR5



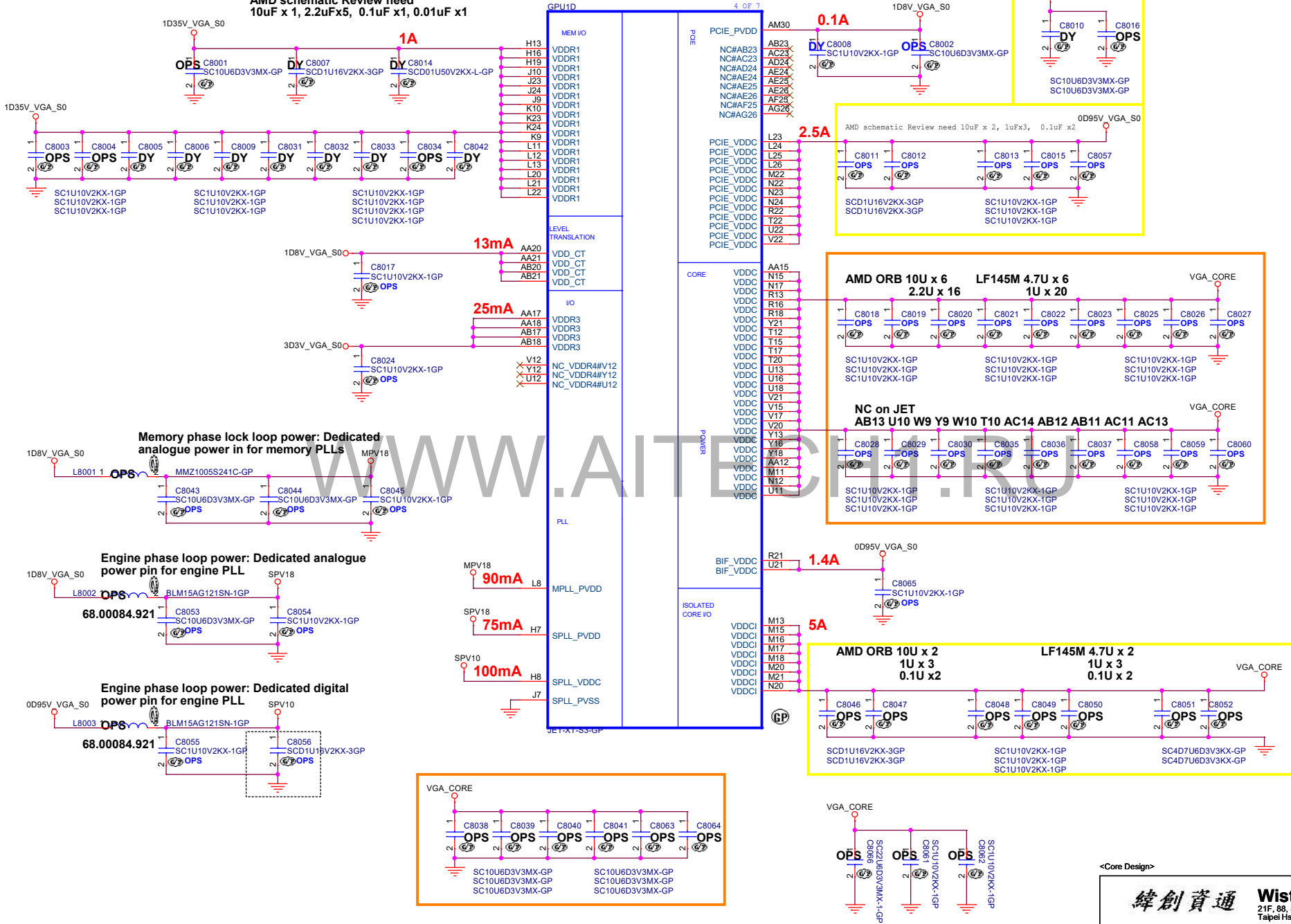
???
Difference with AMD

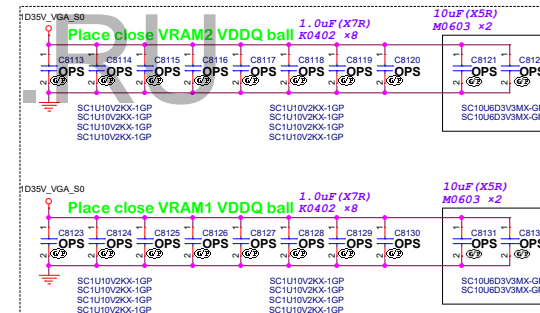
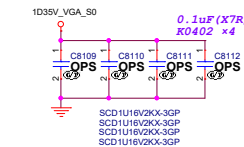
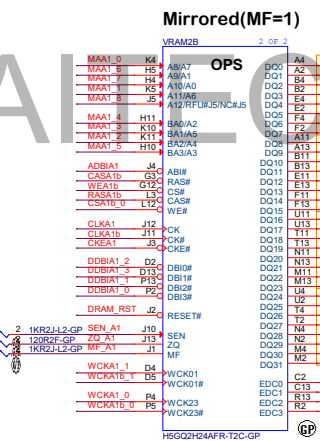
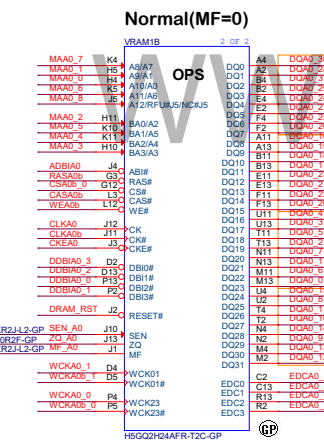
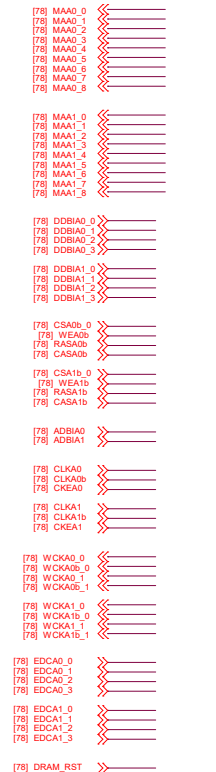


DQ



AMD schematic Review need
10uF x 1, 2.2uF x5, 0.1uF x1, 0.01uF x1






SSID = Vram (GDDR5)

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Title GPU-VRAM3,4 (2/4)		
Size A4	Document Number Turis/Vegas MLK AMD SR/ BR (FP4)	Rev X00
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GPU-VRAM5,6 (3/4)

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GPU-VRAM7,8 (4/4)

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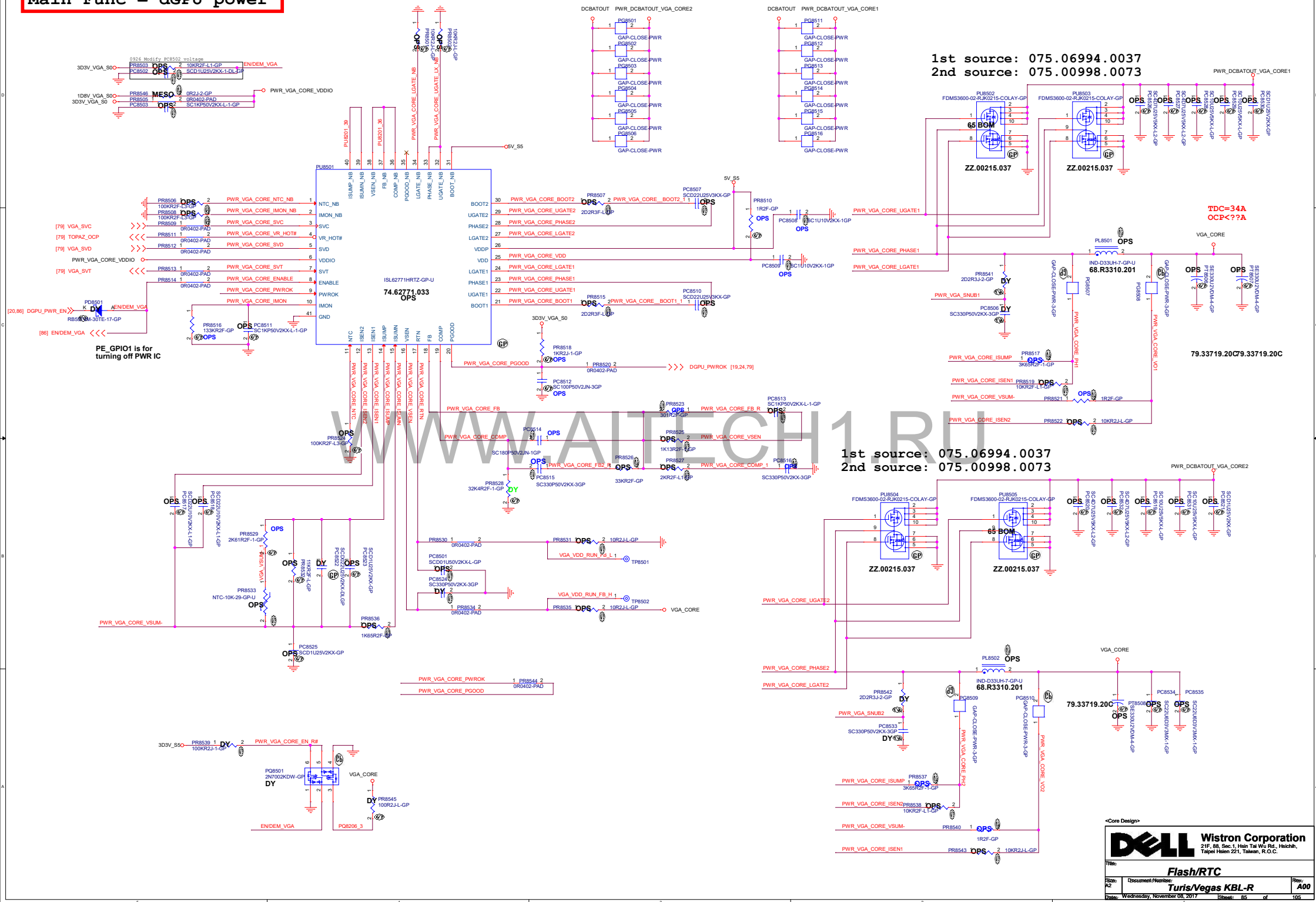
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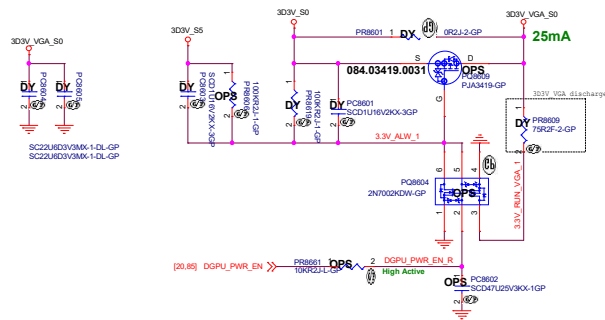
Sheet 84 of 105

Main Func = dGPU power



Main Func = dGPU

3D3V_S0 to 3D3V_VGA_S0 Transfer



GPU PWR Sequencing

3D3V_VGAS0

=> 0D95V_VGA_S0/1D8V_VGA_S0

=> 1D5V_VGA_S0

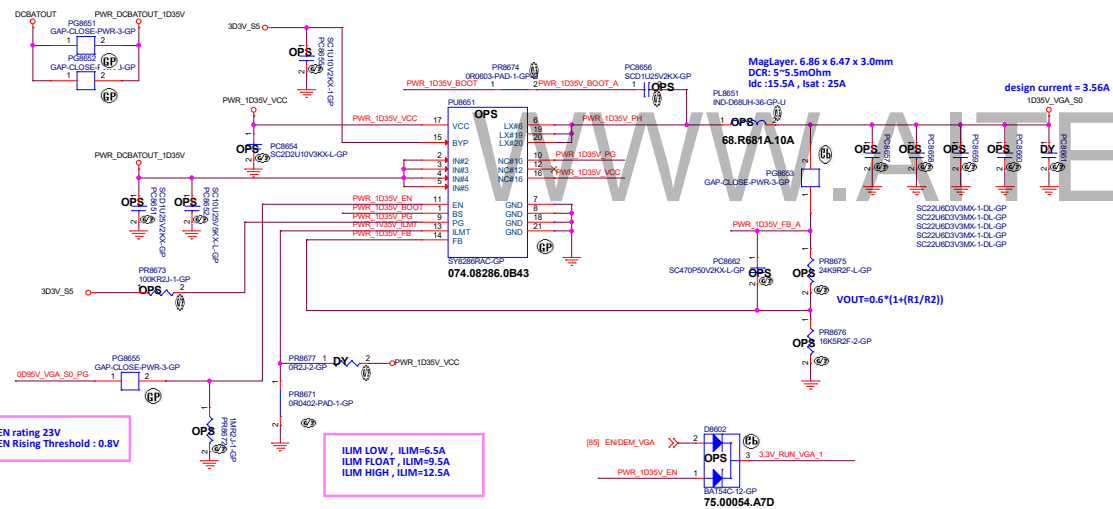
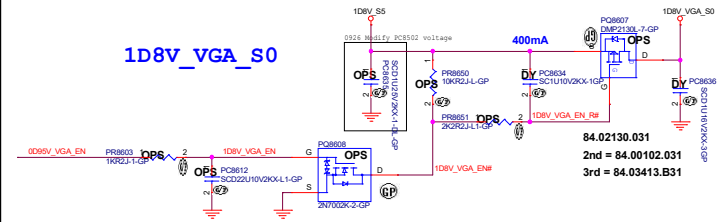
=> VGA_CORE

All the ASIC supplies must reach their respective nominal voltages withing **20ms** of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50mV/us.

It is recommended that the 3.3V rail ramp up first.

It is recommended that the 0.95V rail reach at least 90% of its normal value no later than 2ms from the start of VDDC ramping up.

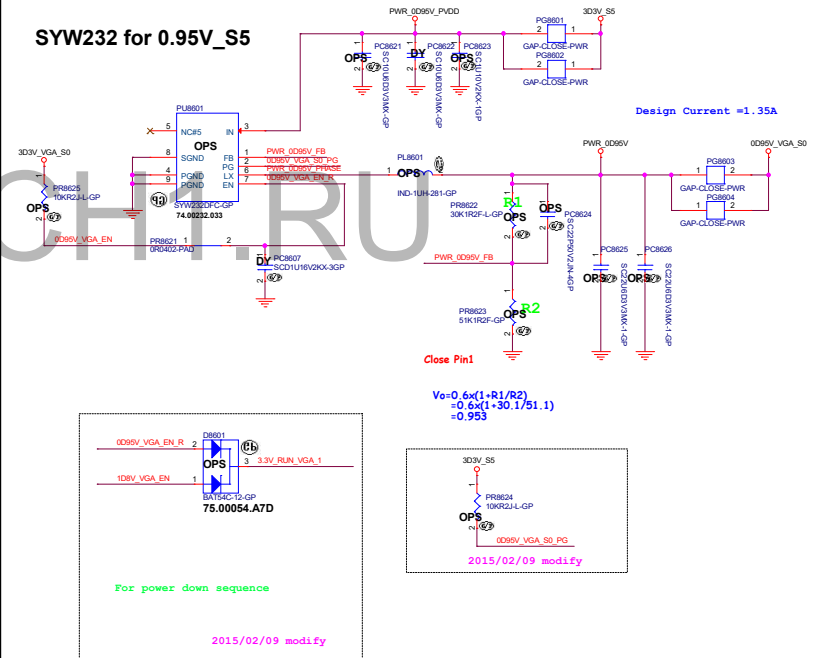
1D8V_VGA_S0



EN rating 23V
EN Rising Threshold : 0.8V

ILIM FLOAT , ILIM=9.5A
ILIM HIGH , ILIM=12.5A

SYW232 for 0.95V_S5


$$\begin{aligned} V_0 &= 0.6 \times (1 + R_1/R_2) \\ &= 0.6 \times (1 + 30.1/51.1) \\ &= 0.953 \end{aligned}$$

2015/02/09 modify

For power down sequence

2015/02/09 modify

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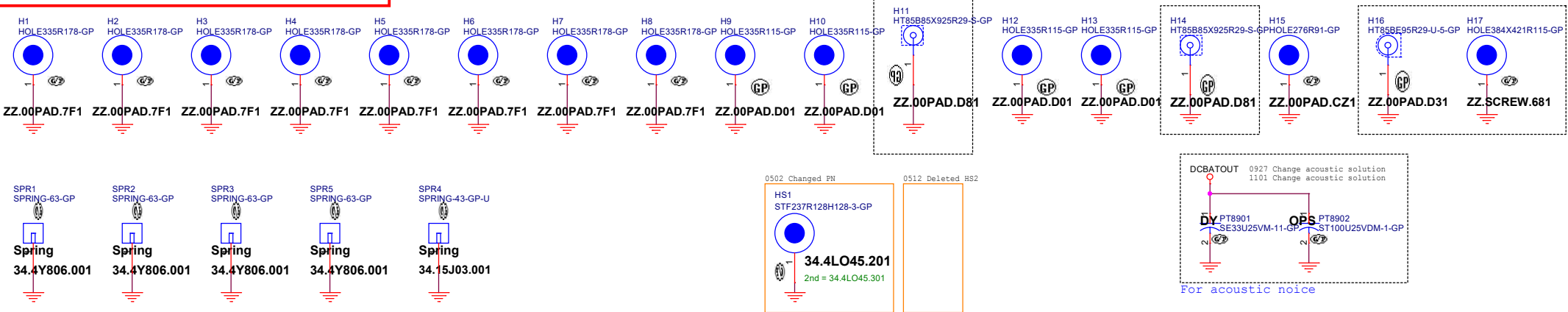
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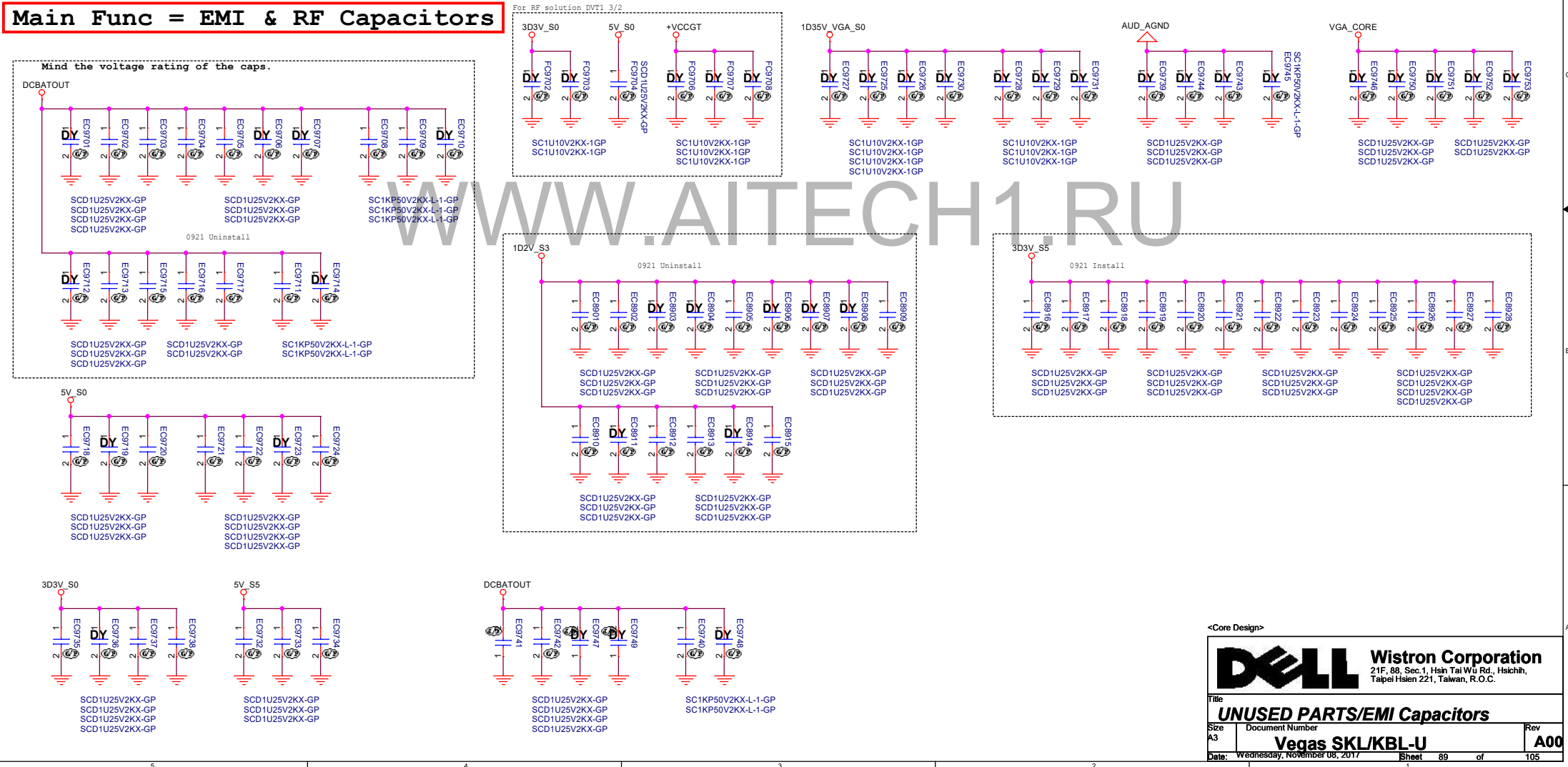
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Main Func = UnusedParts



Main Func = EMI & RF Capacitors



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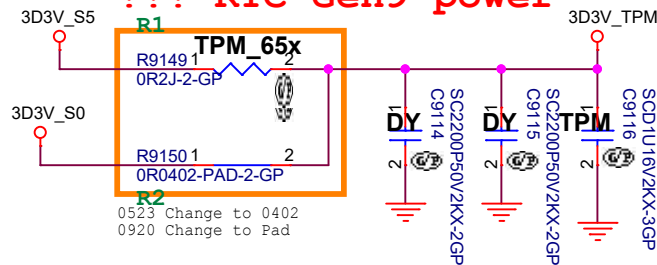
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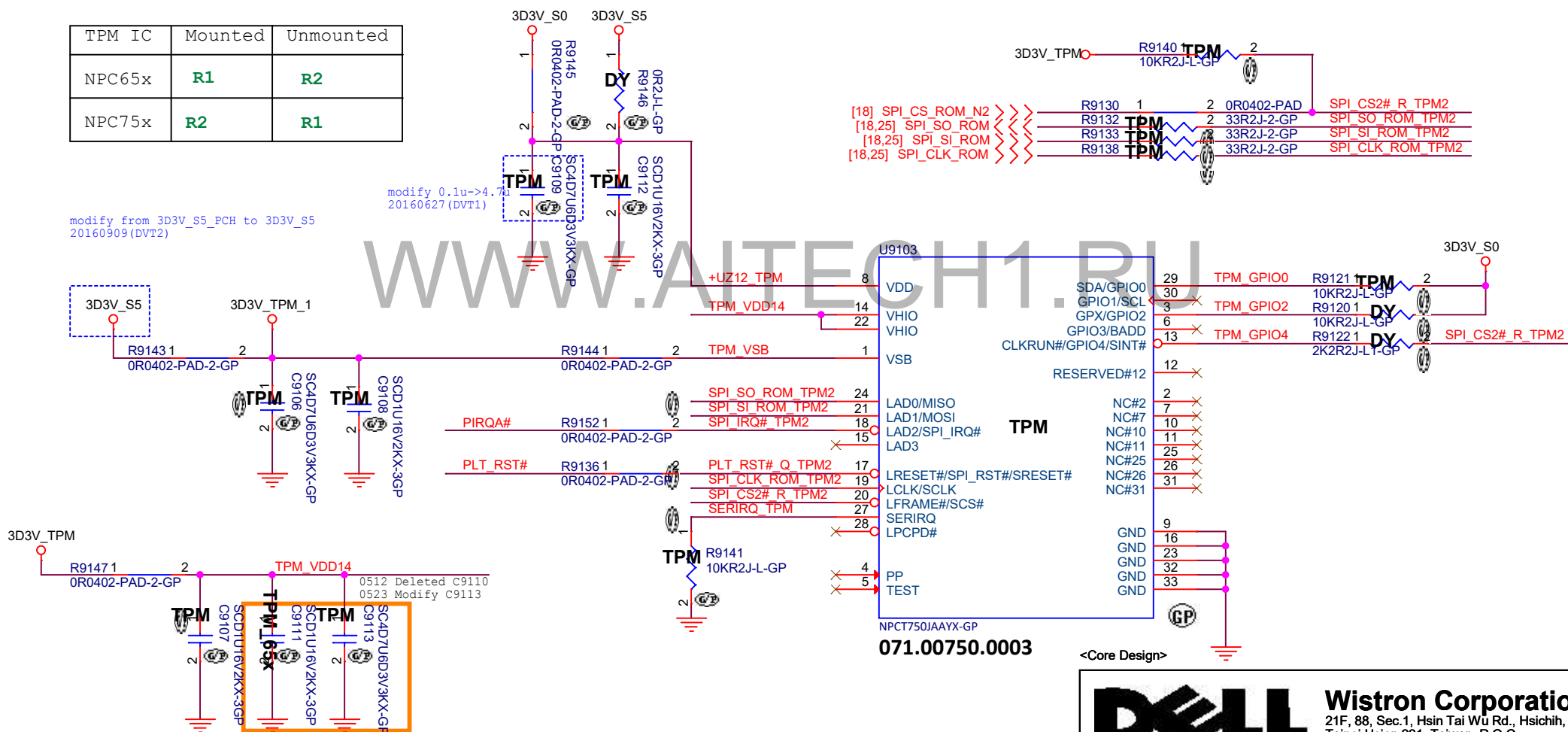
SSID = TPM

??? RTC Gen9 power



TPM IC	Mounted	Unmounted
NPC65x	R1	R2
NPC75x	R2	R1

modify from 3D3V_S5_PCH to 3D3V_S5
20160909 (DVT2)



	NPCT650		NPCT750	
Pin define	Power Name	Power status	Power Name	Power status
Pin1	VSB	VALW	VSB	VALW
Pin8	VDD	VRUN	VHIO	VRUN (S0)
Pin14	VHIO	VSPI	NC	nc
Pin22	VHIO	VSPI	VHIO	VRUN (S0)



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TPM

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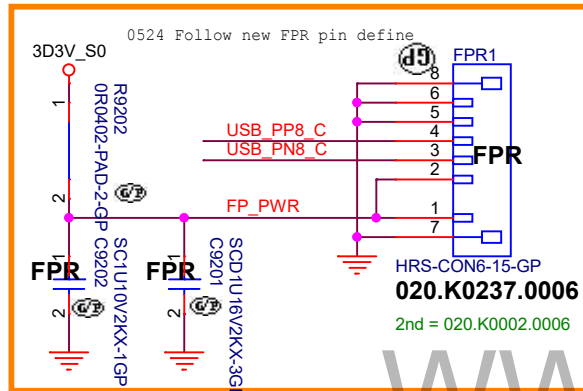
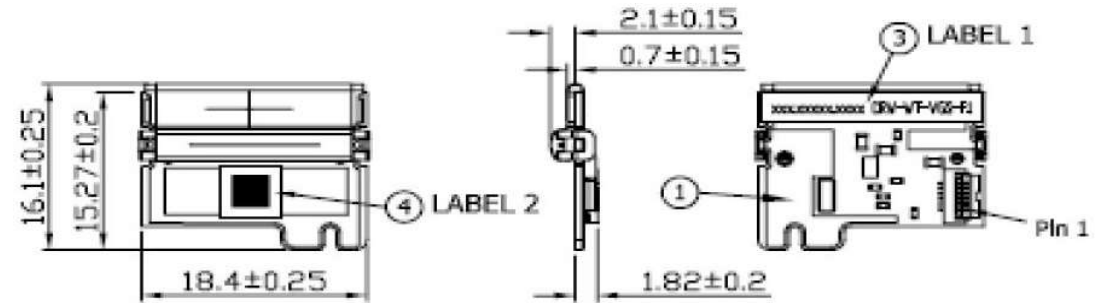
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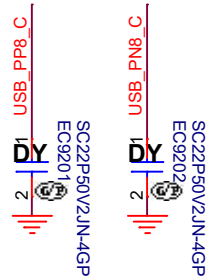
SSID = Finger Print



FingerPrint Pin Assignments.

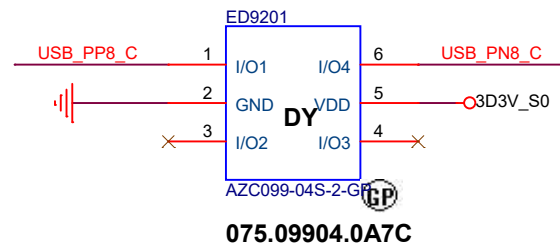
- Pin 1 = 3.3Vin
- Pin 2 = (ND)
- Pin 3 = D-
- Pin 4 = D+
- Pin 5 = Reset_N
- Pin 6 = GND

For EMI Reserved



Layout Note:

close to FPR1



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Title

LVDS_Switch

Size
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Title

CRT Switch

Size

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Document Number

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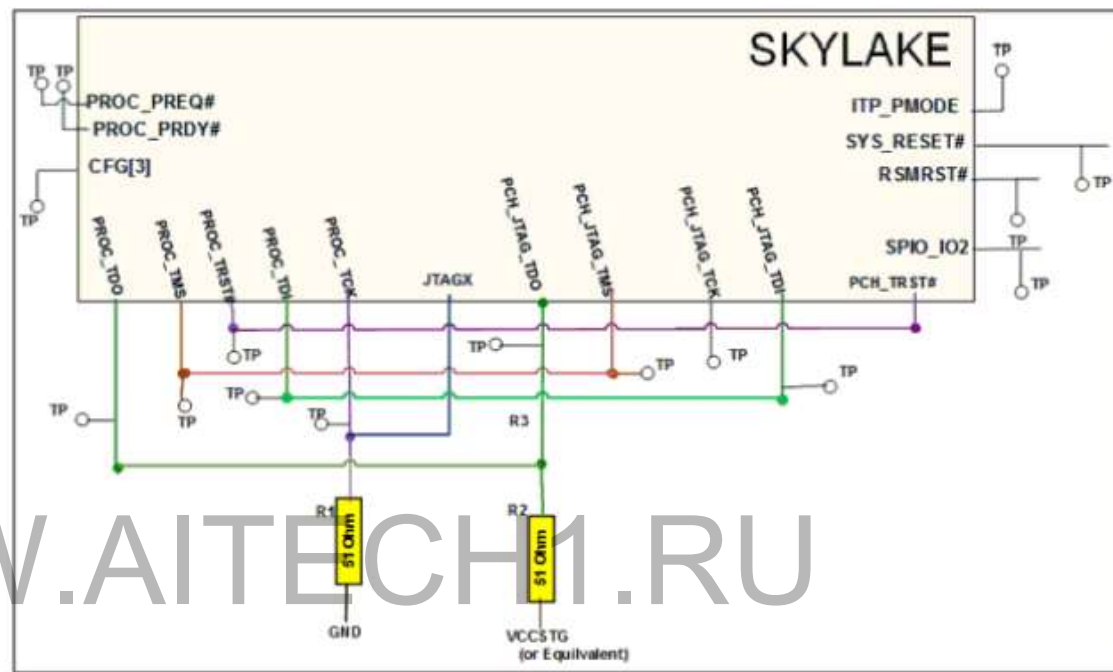
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PCH_JTAG_TMS test point
XDP_TMS test point
PCH_JTAG_TDI test point
XDP_TDI test point
XDP_TCLK test point
XDP_TCK_JTAGX test point
XDP_TDO_CPU test point
PCH_JTAG_TDO test point



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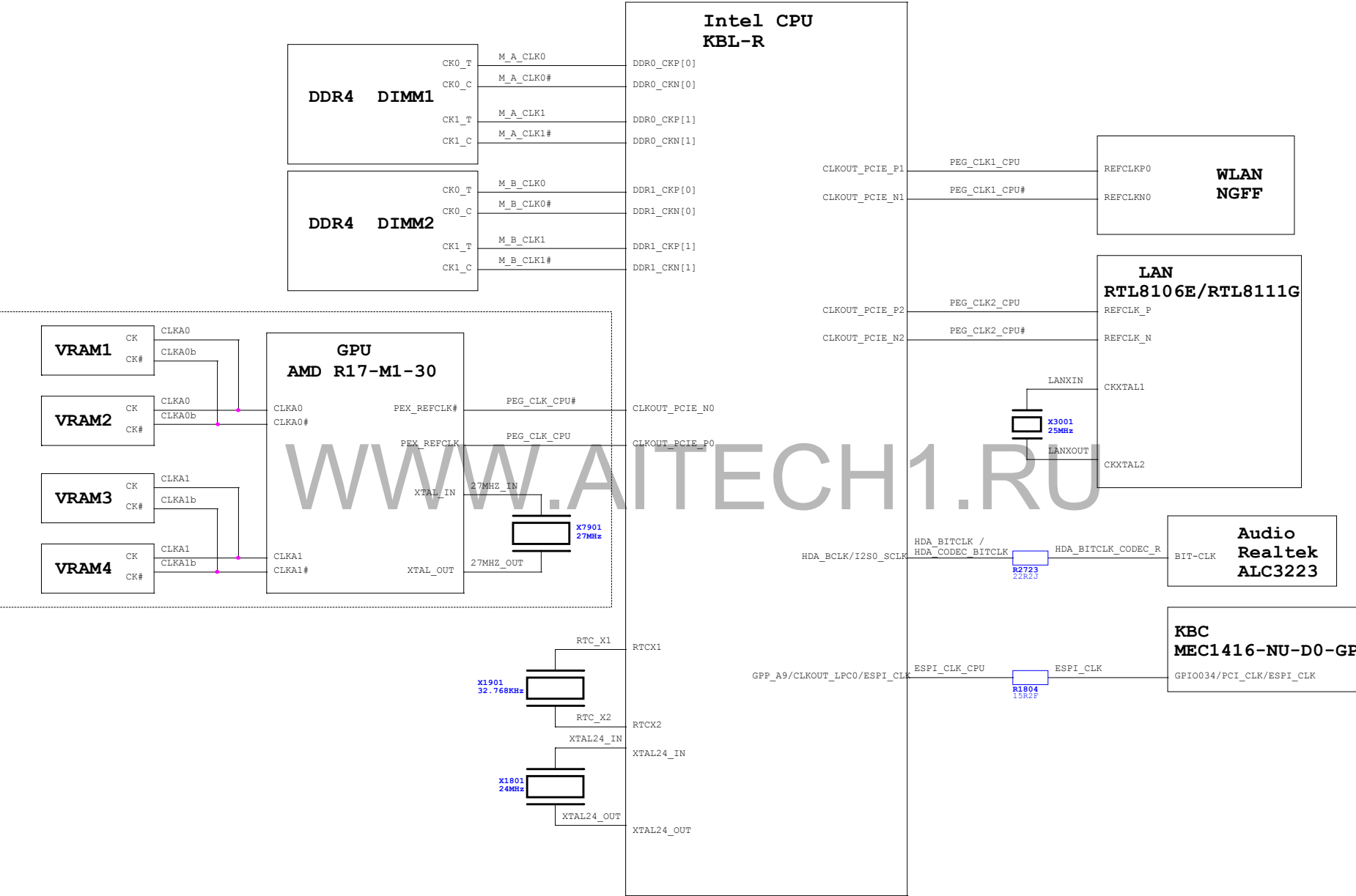
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Title **Debug (XDP debug)**

Size A4 Document Number **Vegas SKL/KBL-U** Rev **A00**

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CLK Block Diagram



[illegible]

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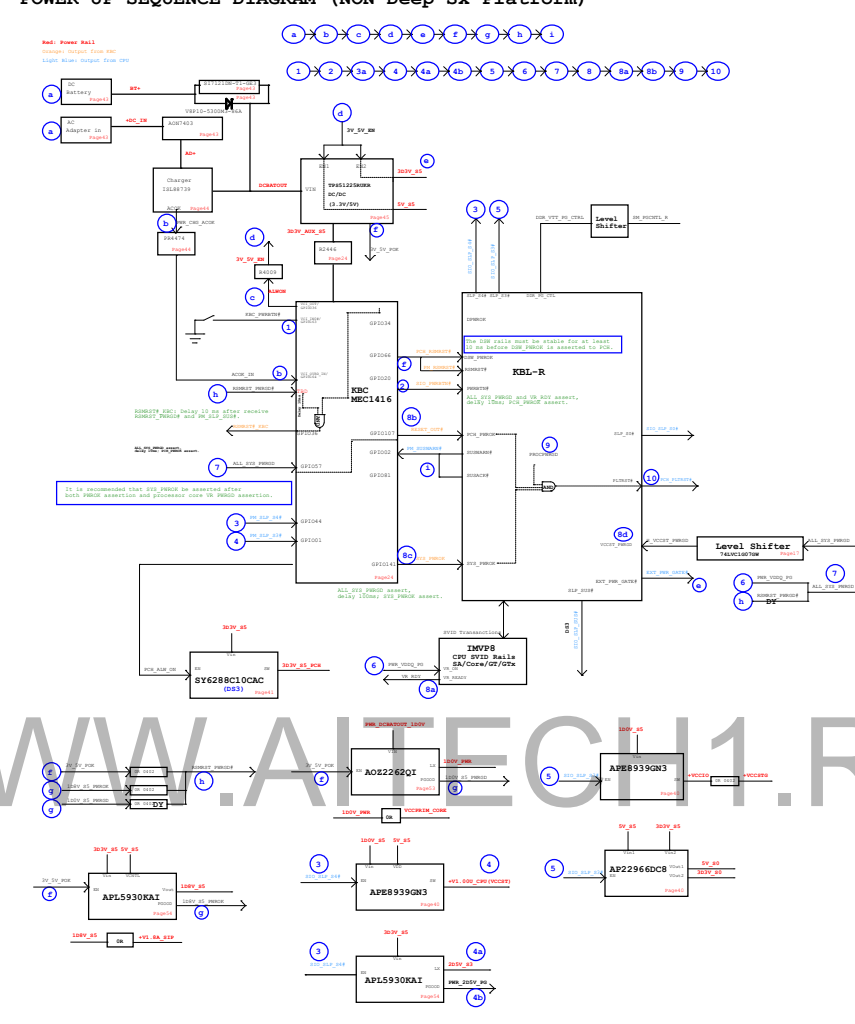


Change History

Vegas SKL/KBL-U

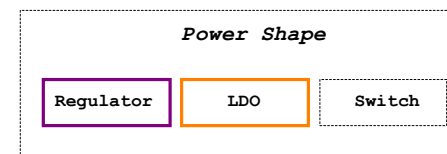
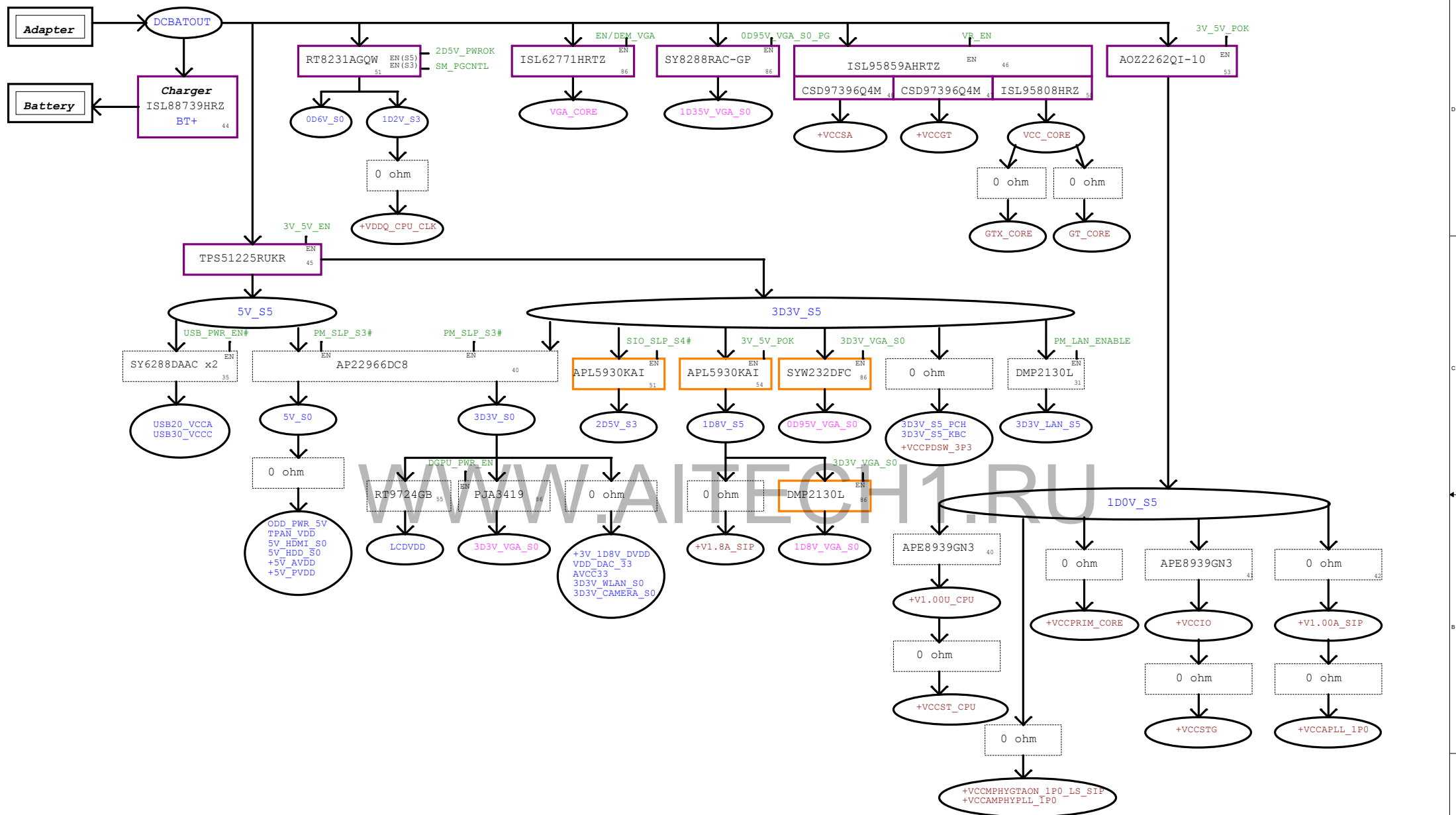
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POWER UP SEQUENCE DIAGRAM (NON Deep Sx Platform)

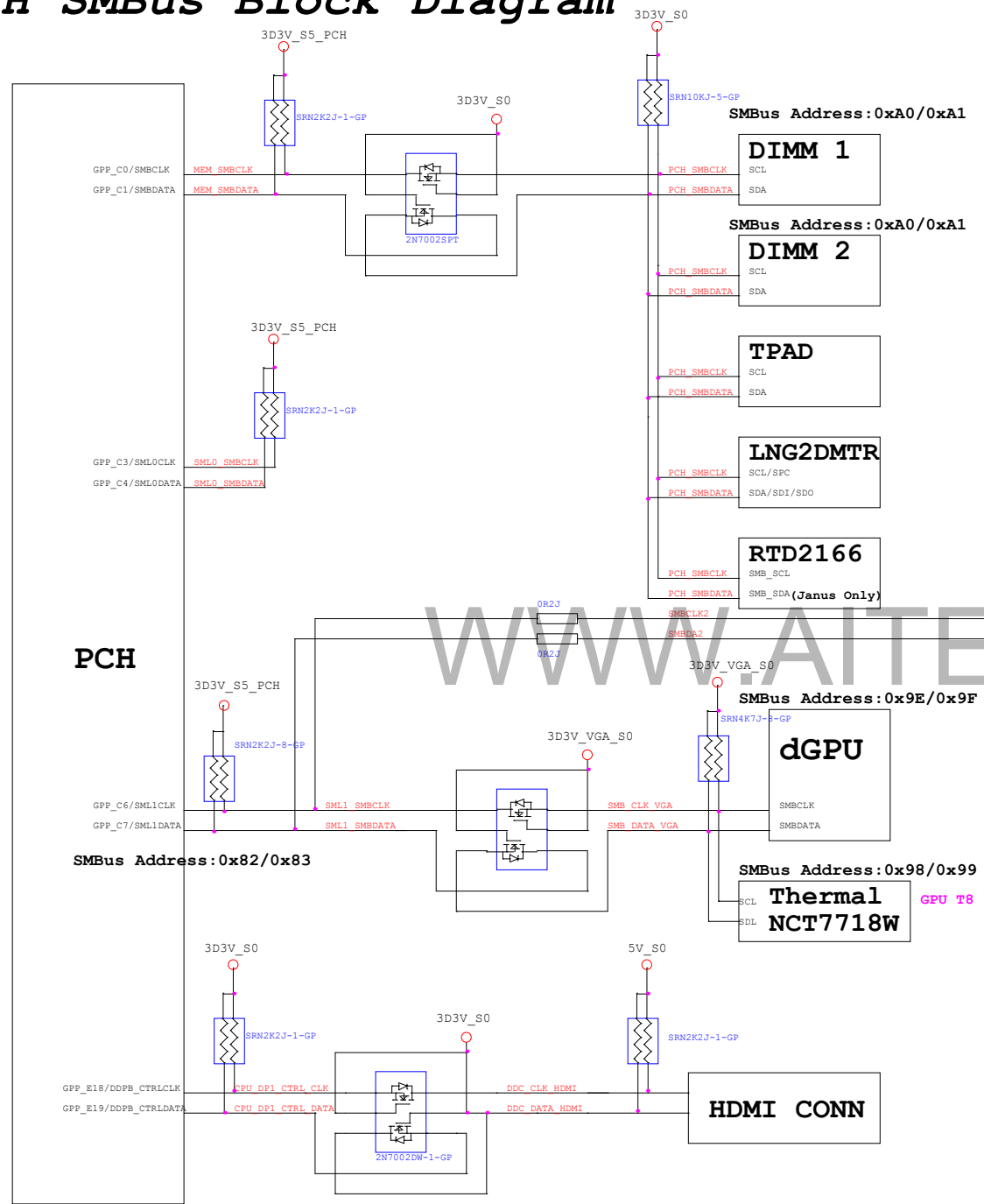


POWER UP RESET SEQUENCE – COLD BOOT

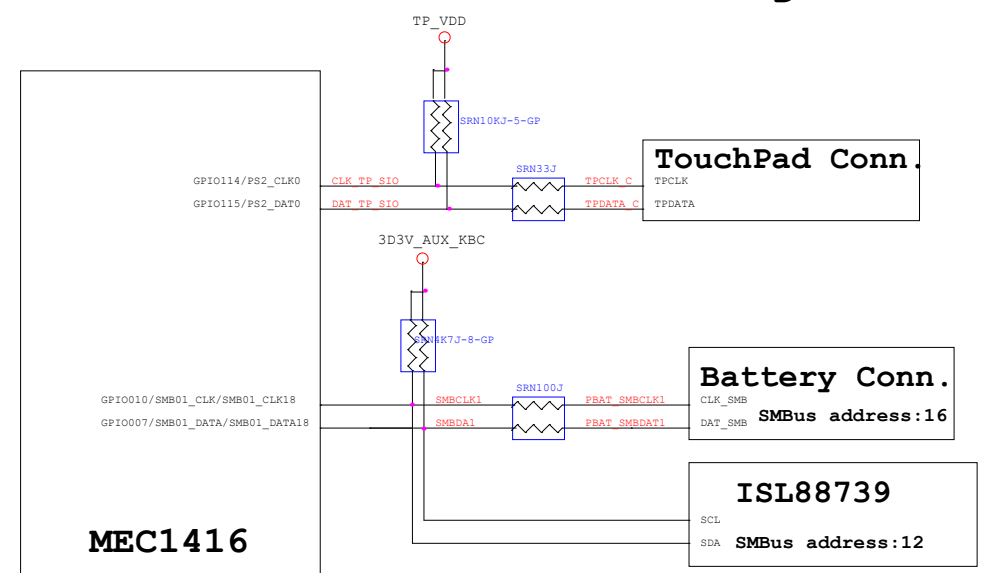




PCH SMBus Block Diagram



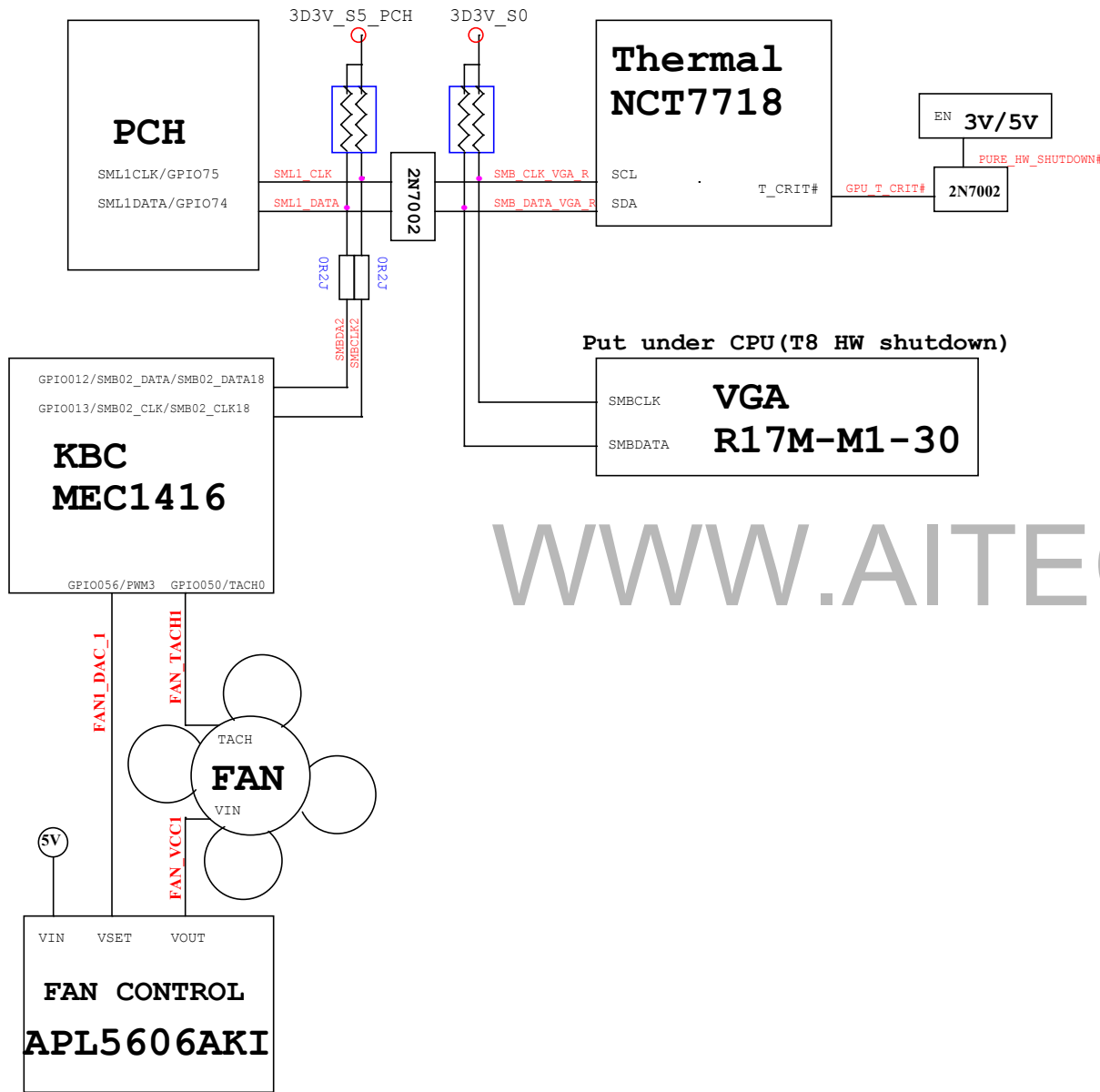
KBC SMBus Block Diagram



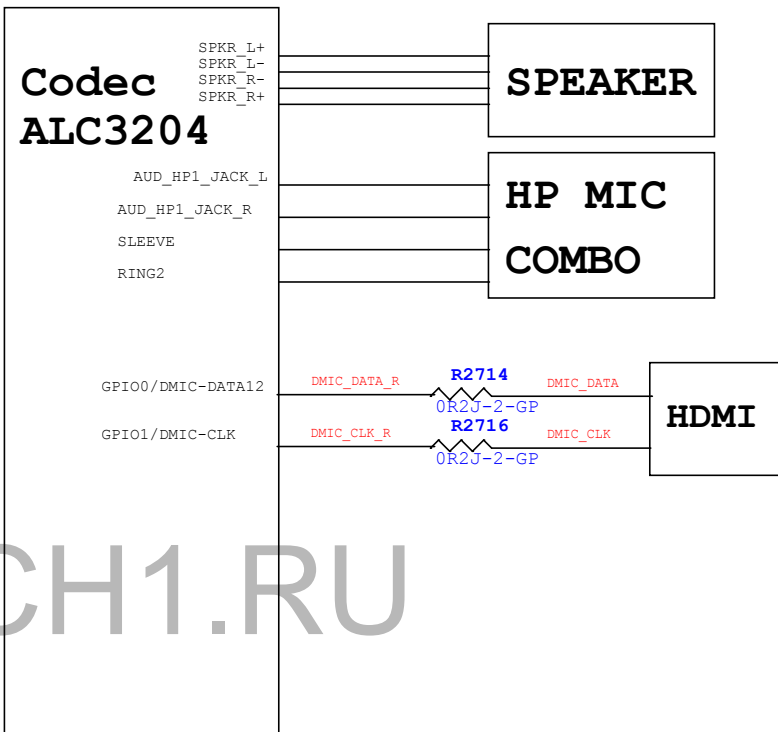
MEC1416

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Thermal Block Diagram



Audio Block Diagram



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<Core Design>